GFEC Stratix II F1020 User's Manual for Development Board

Rev 2.00

UG_EK2SF1020_CHT200

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Any tab or paster on development board should not be torn down or erased, otherwise, it may be disadvantaged to cognizance warrant period of product.

CONTENT

CHARACTERISTICS OVERVIEW OF STRATIX II F1020 DEVELOPMENT BOARD ..... 錯誤! 尚未定義書籤。

1. INTRODUCTION OF THE PRODUCT ..... 錯誤! 尚未定義書籤。

1.1 SPECIFICATIONS OF THE PRODUCTS ..... **錯誤! 尚未定義書籤。**
1.2 PRECAUTIONS ..... **錯誤! 尚未定義書籤。**
1.3 FAST USING THE DEVELOPMENT BOARD ..... **錯誤! 尚未定義書籤。**

2. INFORMATION FOR HARDWARE INSTALLATION... 錯誤! 尚未定義書籤。

2.1. OUTSIDE VIEW OF GFEC EK2SF1020 DEVELOPMENT BOARD . **錯誤! 尚未定義書籤。**
2.2. STRUCTURAL DIAGRAM OF GFEC EK2SF1020 DEVELOPMENT BOARD **錯誤! 尚未定義書籤。**
2.3. DEVICES COMPATIBLE WITH FPGA ..... **錯誤! 尚未定義書籤。**
2.4. POWER SYSTEM ..... **錯誤! 尚未定義書籤。**
2.5. AVAILABLE I/O OF DEVELOPMENT BOARD ..... **錯誤! 尚未定義書籤。**
2.5.1. JP1 & JP5 ..... **錯誤! 尚未定義書籤。**
2.5.2. JP2 & JP6 ..... **錯誤! 尚未定義書籤。**
2.5.3. JP3 & JP7 ..... **錯誤! 尚未定義書籤。**
2.5.4. JP4 & JP8 ..... **錯誤! 尚未定義書籤。**
2.6. SPECIFICATION OF CONFIGURATION EPROM ..... **錯誤! 尚未定義書籤。**
2.7. JTAG ..... **錯誤! 尚未定義書籤。**
2.8. TEST PIN ..... **錯誤! 尚未定義書籤。**
2.9. JUMPER-CHOOSING AREA 33
2.10. DDR SO-DIMM ..... **錯誤! 尚未定義書籤。**
2.11. UART ..... **錯誤! 尚未定義書籤。**
2.12. RE-CONFIGURATION ..... **錯誤! 尚未定義書籤。**
2.13. USAGE OF CLOCK SIGNAL ..... **錯誤! 尚未定義書籤。**
2.14. ELECTRIC SPECIFICATION AND CHARACTERISTICS OF I/O FOLLOW THROUGH SWITCH ..... **錯誤! 尚未定義書籤。**
2.15. SYSTEM STATUS INDICATORS ..... **錯誤! 尚未定義書籤。**
2.16. STACKING ..... **錯誤! 尚未定義書籤。**

3. INFORMATION ABOUT SOFTWARE ..... 錯誤! 尚未定義書籤。

3.1. QUARTUSII VERSION SUPPORT ..... **錯誤! 尚未定義書籤。**
3.2. VERSION SUPPORT FROM COOPERATION MANUFACTURER . **錯誤! 尚未定義書**

籤。
3.3. SOFTWARE OPERATION .....錯誤! 尚未定義書籤。
3.3.1. JTAG .....錯誤! 尚未定義書籤。
3.3.2. ACTIVE SERIAL PROGRAMMING (AS) .....錯誤! 尚未定義書籤。
4. APPENDIX ..... 錯誤! 尚未定義書籤。
4.1. GUIDE FOR INSTALLING BYTE BLASTER MV/II IN WINDOWS 2K/XP .錯誤! 尚未定義書籤。
4.2. DODIFY THE COMPATIBILITY OF MICROSOFT WINDOW XP SP2 ..錯誤! 尚未定義書籤。
4.3. DIMENSIONAL DRAWING .....錯誤! 尚未定義書籤。
4.4. SCHEMATIC .....錯誤! 尚未定義書籤。
4.5. I/O BUFFER SPEC .....錯誤! 尚未定義書籤。
5. REFERENCE .....錯誤! 尚未定義書籤。
VERSION CHANGE RECORD ..... 錯誤! 尚未定義書籤。

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Characteristics Overview of Stratix II F1020 Development Board

50% Faster Performance
2.25X Logic Capacity Increase
40% Lower Price per Density
4X DSP Bandwidth Increase
1-Gbps LVDS
New, Faster External Memory Interfaces
Non-Volatile Design Security
TriMatrix™ Memory
Digital Signal Processing Blocks
External Memory Interfaces
840-Mbps Differential I/O Pins
Remote System Upgrades

1. Introduction of the product

The development board is designed for IC development and verification, therefore, it is compatible with Altera Stratix II Device Family. FPGA of EP2S180F1020 of the largest specification can provide embedded memory with a maximum capacity of 179,400 LEs, 9,383,040 bits and maximum 753 available I/Os for IC designers. If the FPGA of maximum capacity still can't meet design requirement, you can extend the available capacity by means of stacking.

FPGA performance reaches new heights with the Stratix® II device family—the industry's fastest and highest-density FPGAs. Built on a new and innovative logic structure, Stratix II devices on average deliver 50 percent higher performance and offer more than twice the logic capacity of first-generation Stratix FPGAs. Stratix II devices extend the possibilities of FPGA design, allowing designers to meet the high-performance requirements of today's advanced systems and avoid developing with costly ASICs. Based on the award-winning Stratix device family architecture, Stratix II devices are outfitted with a powerful set of system-level features and incorporate many significant enhancements and new capabilities.

Stratix II FPGAs are manufactured on 300-mm wafers using TSMC's 90-nm, low-k dielectric process technology. Stratix II devices mark the debut of an innovative and efficient logic structure that maximizes performance while consuming fewer resources and provides full backward compatibility with previous-generation architectures. This logic structure increases device densities to never-before-seen levels, reaching up to 180K equivalent logic elements (LEs) and 9 Mbits of RAM, all at a significantly lower cost than prior-generation FPGAs.

Stratix II devices were designed in concert with the Quartus® II software to deliver unmatched performance and ease of use. The Quartus II software is the industry's most advanced development software for high-density FPGAs and provides a comprehensive suite of synthesis, optimization, and verification tools in a single, unified design environment.

Stratix II FPGAs are ideal for prototyping ASICs. Providing the highest density and the highest performance, Stratix II can emulate and validate an ASIC design with the high performance and density expected to model an ASIC accurately.With support for migration to HardCopy® II structured ASICs, Stratix II FPGAs offer the industry's only seamless development path from FPGA prototype to high-volume, structured ASIC production. Designing with HardCopy II devices allows users to reduce development costs and still get the flexibility and time-to-market advantages associated with FPGAs.

Top-level function

Stratix II devices improve on the features that set new standards in FPGAs (shown in Figure 1). New device capabilities such as the new logic structure and design security technology round out the industry's most advanced FPGA feature set.

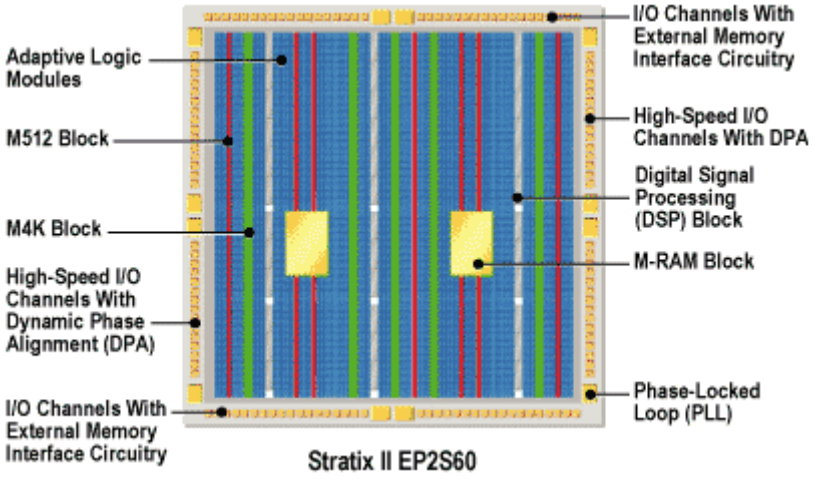


Fig. 1 Stratix II EP2S60 Floorplan

New Logic Structure

- New and innovative logic structure based on adaptive logic modules (ALMs) packs more logic into less area and enables higher performance.
- Dedicated arithmetic functionality to efficiently implement adder trees and other computationally intensive functions

High-Speed I/O Signaling & Interfaces

- 1-Gbps source-synchronous I/O signaling performance in dedicated serialization/deserialization (SERDES) circuitry
- Dynamic phase alignment (DPA) circuitry accelerates maximum performance by dynamically resolving external board and internal device skew
- Support for differential I/O signaling levels, including HyperTransport™ technology, LVDS, LVPECL, and differential SSTL and HSTL.

External Memory Interfaces

- Support for the latest external memory interfaces in dedicated circuitry, including DDR2 SDRAM, RLDRAM II, and QDRII SRAM devices
- Sufficient bandwidth and I/O pins to support interfacing with multiple, standard 64-bit or 72-bit, 168-/144-pin DIMMs.

Design Security

- Brings programmable logic functionality and benefits to new applications requiring design security

- 128-bit advanced encryption standard (AES) design security using configuration bitstream encryption technology
- Key securely stored in FPGA and does not require battery backup or consume logic resources

TriMatrix™ Memory

- Up to 9 Mbits of memory in three block sizes: M-RAM, M4K, and M512 blocks.
- Includes parity bits for error checking.
- Performance up to 400 MHz.
- Mixed-width data and mixed-clock modes

Digital Signal Processing (DSP) Blocks

- More DSP block bandwidth with up to 4x more DSP bandwidth than Stratix devices.
- Dedicated multiplier, pipeline, and accumulate circuitry
- New rounding and saturation support in Q1.15 format in each DSP block
- Maximized performance of up to 420 MHz

Clock Management Circuitry

- Up to 12 on-chip phase-locked loops (PLLs) for device and board clock management
- Dynamic PLL reconfiguration allowing on-the-fly PLL parameter changes.
- Redundant clock switchover for error recovery and multi-clock systems

On-Chip Termination

- On-chip, differential, and series termination reducing board design complexity and cost

Remote System Upgrades

- Remote system upgrades for reliable and safe deployment of in-system upgrades and bug fixes
- Dedicated watchdog circuitry ensures proper functionality after update.

1.1 Specifications of the Products

When you get the GFEC EK2SF1020 development board package, please check its content according to the following:

☑StratixII Development Board , 1pec.
☑ADAPTER, 1 pec. (power supply converter for AC 110V/220V to DC 6V/3A)
☑ Power Cable, 1 set (red and white)
☑USB Download Cable, 1 pec.
☑CD-ROM
☑Special Connector, 4 pecs.
☑Head Sink for Stratix II

If you find any part absent or any damage to them, please contact GFEC as soon as possible.

1.2 Precautions

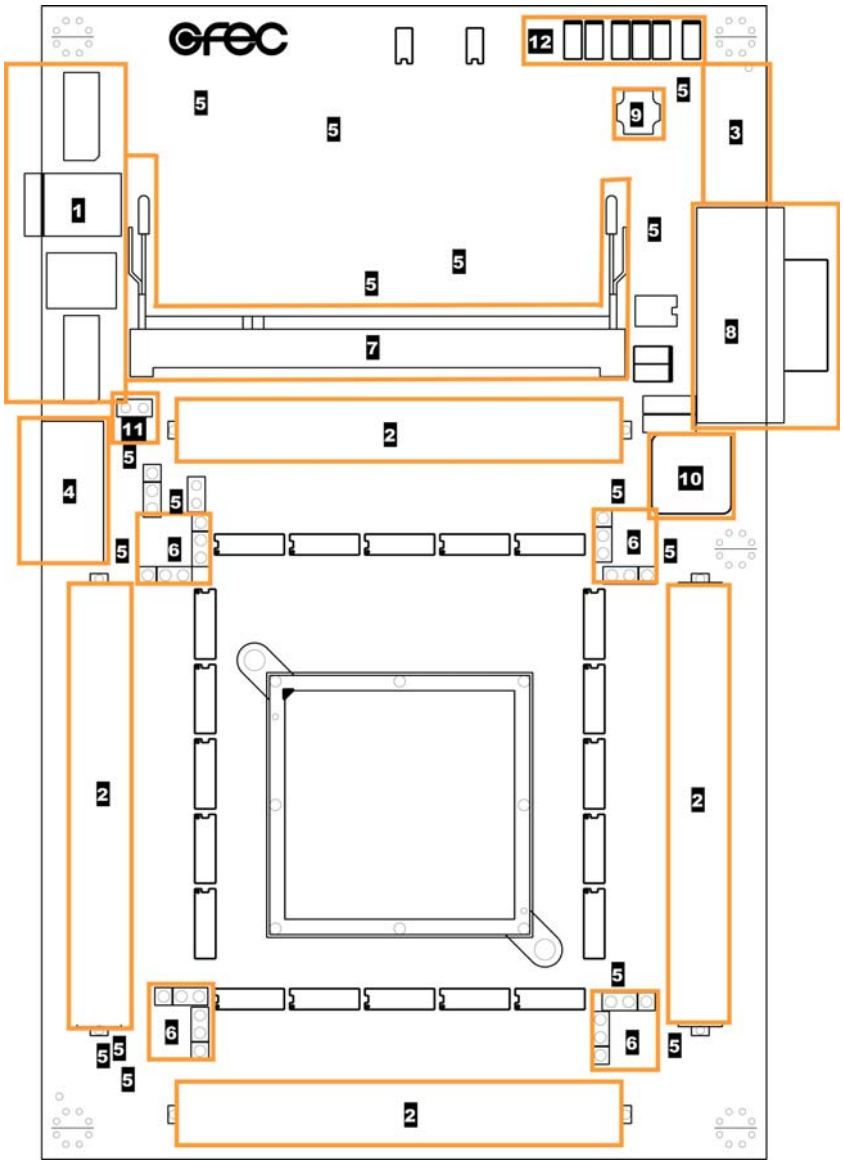
The development board is made up of lots of precise integrated circuits and their components. Since these circuits easily subject to damage due to electrostatic influence, please read the user's manual carefully and do the following preparation before installation.

- If you find any pin bendding or it's not easy to insert before inserting the development into the system designed by yourself, you should not insert it by force. Otherwise, we can't offer warranty to the damaged pin caused by doing so.
- You should not insert or pull out over frequently or with over force when the board were connected. It is helpful to prolong service life of pins. The board should be inserted or pulled out slowly in all direction so as to avoid pins being bent.
- Please confirm the voltage of power supply and wiring once again before you turn the power on.
- If the ISP function is needed, you should connect the development board and Byteblaster II, USB Blaster or Byteblaster MV Download Cable before you turn the power on.
- You should avoid contacting metal wires and main body of IC package as possible as you can when you take the development board.
- If it is necessary for you to contact the IC board with your hand, you should wear antistatic gloves to avoid the board subjecting to destroy or damage
- When the development board is not installed or used, it should be placed on an antistatic mat or kept in an antistatic pocket.
- Please confirm that all points are set correctly before turning the power on.
- Check supply voltage and wirings for several times before turning the power on.
- The board must not be thrown down or collided. Any conducting material should not contact with any wiring or parts on the PCB board. If you find the development board is damaged obviously, you must not power up the board to test, otherwise it will result in danger and IC destroy or damage.
- If you need to stack the development board to expand its capacity, please confirm whether there is any conflict happened in I/O settings,

so as to avoid damage the follow through switch.

- Operators should wear static-prevent devices.
- On the related limitations and characteristics of Altera device used in this product, please refer to Altera Data Manual.
- All adjustable points of this product are set with removable jumper. Users should not change them by themselves.
- Power cable and download cable are expected as short as possible, so as to reduce noise.
- If you have any question to the product, be sure to consult our engineers before you use it, so as to avoid damage by improper operation.

1.3 Fast Using the Development Board



1.	Power System	Detail See 2.4	2.	Extension Connector	Detail See 2.5
3.	AS Configuration	Detail See 2.6	4.	JTAG Configuration	Detail See 2.7
5.	Test Ping	Detail See 2.8	6.	B1~B8 Bank Voltage	Detail See 2.9
7.	DDR SDRAM	Detail See 2.10	8.	UART	Detail See 2.11
9.	Re-Download	Detail See 2.12	10.	Oscillator Socket	Detail See 2.13
11.	FAN Connector	Detail See 2.14	12.	System Status Indicators	Detail See 2.16

2. Information for Hardware Installation

2.1. Outside View of GFEC EK2SF1020 Development Board

The following is the outside view of GFEC Stratix II development board in its actual size.

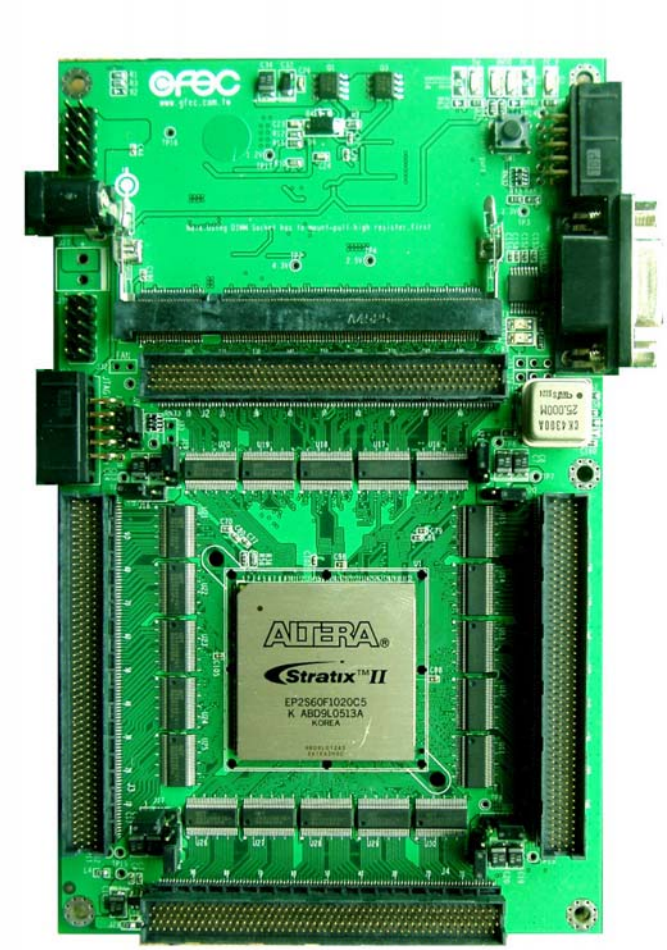


Fig. 2 outside view of GFEC Stratix II development board

2.2. Structural Diagram of GFEC EK2SF1020 Development Board

The following is the structural diagram of GFEC Stratix II development board in its actual size:

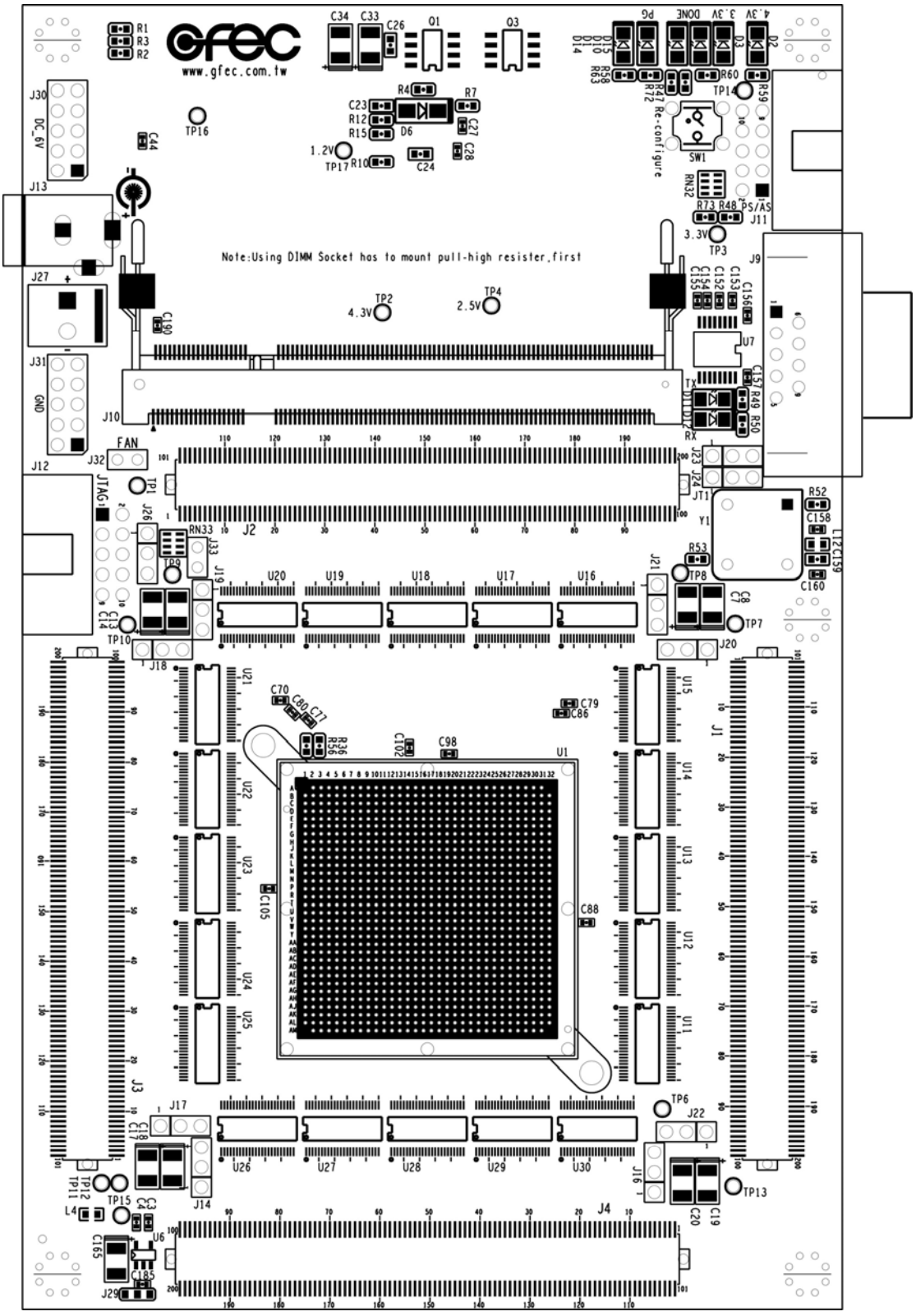


Fig. 3 structural diagram of GFEC Stratix II development board

2.3. Devices compatible with FPGA

All specifications of devices that are compatible with Stratix II Device Family are listed in the following table2-1. The development board supports the devices above EP2S60.

Device	ALMs	Equivalent LEs	M512 Blocks	M4K Blocks	M-RAM Blocks	Total Memory Bits	DSP Blocks	18x18 Multipliers	PLLs
EP2S15	6,240	15,600	104	78	0	419,328	12	48	6
EP2S30	13,552	33,880	202	144	1	1,369,728	16	64	6
EP2S60	24,176	60,440	329	255	2	2,544,192	36	144	12
EP2S90	36,384	90,960	488	408	4	4,520,448	48	192	12
EP2S130	53,016	132,540	699	609	6	6,747,840	63	252	12
EP2S180	71,760	179,400	930	768	9	9,383,040	96	384	12

Tab. 1 Stratix Device Family

All packages supported by IC of Stratix II Device Family and available I/Os are listed in table 2.2. The package which can be supported by the development board is Fine-BGA 1020 Pin.

Device	F484	H484	F672	F780	F1020	F1508
EP2S15	341		365			
EP2S30	341		499			
EP2S60	341		499		717	
EP2S90		308		534	757	901
EP2S130				534	741	1,109
EP2S180					741	1,173

Tab. 2 Stratix II Package Offerings & Users I/O Counts

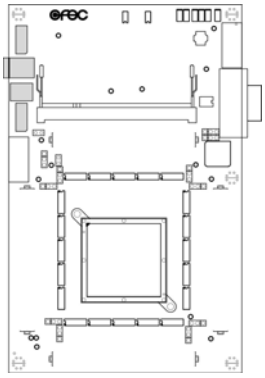
2.4. Power System

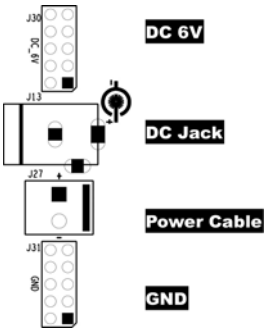
The development board can be supplied power with the adapter attached. The adapter can also accept DC 6V input supplied by the user if no proper

power source can supply to the adapter or the required power consumption is higher than the attached adapter in the using location.

The board contains power process circuit. There are three ways to input power, each of them are described in the following:

- We offer special adapter for our customers. It can transform AC110V/240V into DC6V, can be connected on J13 directly, providing necessary power to the board. But it just can be used in the systems lower than 3A. If there is any special requirement by the system, the power for the outside should be supplied additionally.
- Connect the DC power adapter with the double cables attached after check positive and negative poles. The input voltage is DC6V.
- The board can be used with other board together. In this case, the power is supplied from the other board, but it must be lower than DC 6V.





2.5. Available I/O of Development Board

The development board sends all I/Os available to FPGA from follow through switch to connector, to ensure all I/Os of FPGA not to be destroyed by extra high external voltage or current. Detailed information of follow through switch sees the appendix. When the board is used to validate circuit, we recommend to use the user I/O of EP2S60F1020 mainly, so as to avoid changing different size FPGA in F1020 at will.

The development board is pre-set as PLL Enable. If it is required to disable the embedded PLL for saving electricity or others, the pll_ena pin should be controlled by extrinsic loop.

The followings explain pins with special input.

Pin Name	Optional Function	Bank	Location	Board Location
CLK0p	Input/Output	B2	T32	JP1.44

CLK0n	Input/Output	B2	T31	JP1.45
CLK1p	Input	B2	T30	JP1.46
CLK1n	Input	B2	T29	JP1.47
CLK2p	Input/Output	B1	U32	JP1.52
CLK2n	Input/Output	B1	U31	JP1.53
CLK3p	Input	B1	U30	JP1.54
CLK3n	Input	B1	U29	JP1.55
CLK4p	Input/Output	B8	AM17	JP4.46
CLK4n	Input/Output	B8	AL17	JP4.47
CLK5p	Input/Output	B8	AK17	JP4.48
CLK5n	Input/Output	B8	AJ17	JP4.49
CLK6p	Input/Output	B7	AM16	JP4.52
CLK6n	Input/Output	B7	AL16	JP4.53
CLK7p	Input/Output	B7	AH16	JP4.56
CLK7n	Input/Output	B7	AG16	JP4.57
CLK8p	Input/Output	B6	U1	JP3.44
CLK8n	Input/Output	B6	U2	JP3.45
CLK9p	Input	B6	U3	JP3.46
CLK9n	Input	B6	U4	JP3.47
CLK10p	Input/Output	B5	T1	JP3.52
CLK10n	Input/Output	B5	T2	JP3.53
CLK11p	Input	B5	T3	JP3.54
CLK11n	Input	B5	T4	JP3.55
CLK12p	Input/Output	B4	A16	JP2.44
CLK12n	Input/Output	B4	B16	JP2.45
CLK13p	Input/Output	B4	E16	JP2.48
CLK13n	Input/Output	B4	F16	JP2.49
CLK14p	Input/Output	B3	A17	JP2.54
CLK14n	Input/Output	B3	B17	JP2.55
CLK15p	Input/Output	B3	C17	JP2.56
CLK15n	Input/Output	B3	D17	JP2.57
FPLL7CLKp	Input	B2	D30	JP1.4
FPLL7CLKn	Input	B2	D29	JP1.5
FPLL8CLKp	Input	B1	AJ30	JP1.98
FPLL8CLKn	Input	B1	AJ29	JP1.99
FPLL9CLKp	Input	B6	AJ3	JP3.4
FPLL9CLKn	Input	B6	AJ4	JP3.5

FPLL10CLKp	Input	B5	D3	JP3.98
FPLL10CLKn	Input	B5	D4	JP3.99
TDI	Input(Configuration)	B8	AL13	JP4.102
TMS	Input(Configuration)	B8	AE24	JP4.109
TCK	Input(Configuration)	B8	AF24	JP4.110
TDO	Output(Configuration)	B4	C8	JP2.2
PLL_ena	Input	B7	AF8	JP4.196
TMEPDIODEp	Input		G9	JP2.152
TMEPDIODEn	Input		B3	JP2.153

Tab. 3 Dedicate Pin

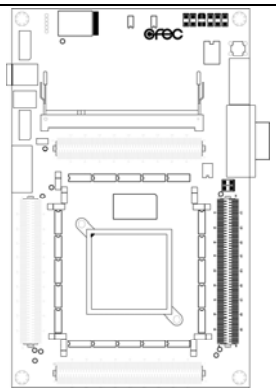
Pin Name	EP2S60	EP2S90	EP2S130	EP2S180	Board Location
AC29	NC	I/O	I/O	I/O	JP1.75
AC30	NC	I/O	I/O	I/O	JP1.74
AD3	NC	I/O	I/O	I/O	JP3.22
AD4	NC	I/O	I/O	I/O	JP3.23
AD29	NC	I/O	I/O	I/O	JP1.79
AD30	NC	I/O	I/O	I/O	JP1.78
AE5	NC	I/O	I/O	I/O	JP3.106
AE6	NC	I/O	I/O	I/O	JP3.107
AE9	NC	I/O	Reserve	Reserve	JP4.193
AF5	NC	I/O	Reserve	Reserve	JP3.104
AF6	NC	I/O	Reserve	Reserve	JP4.105
AF14	NC	I/O	Reserve	Reserve	JP4.157
AF27	NC	I/O	Reserve	Reserve	JP1.199
AF28	NC	I/O	Reserve	Reserve	JP1.198
AG21	NC	I/O	Reserve	Reserve	JP4.121
AG25	NC	I/O	Reserve	Reserve	JP4.106
F21	NC	I/O	Reserve	Reserve	JP2.71
F25	NC	I/O	Reserve	Reserve	JP2.198
G5	NC	I/O	I/O	I/O	JP3.198
G6	NC	I/O	I/O	I/O	JP3.199
G14	NC	I/O	Reserve	Reserve	JP2.138
G27	NC	I/O	I/O	I/O	JP1.105
G28	NC	I/O	I/O	I/O	JP1.104
H3	NC	I/O	I/O	I/O	JP3.82

H4	NC	I/O	I/O	I/O	JP3.83
H5	NC	I/O	Reserve	Reserve	JP3.196
H6	NC	I/O	Reserve	Reserve	JP3.197
H9	NC	I/O	Reserve	Reserve	JP2.123
J29	NC	I/O	I/O	I/O	JP1.23
J30	NC	I/O	I/O	I/O	JP1.22
L27	NC	I/O	Reserve	Reserve	JP1.115
L28	NC	I/O	Reserve	Reserve	JP1.114
N10	NC	I/O	I/O	I/O	JP3.174
N11	NC	I/O	I/O	I/O	JP3.175
P22	NC	I/O	I/O	I/O	JP1.139
P23	NC	I/O	I/O	I/O	JP1.138
W10	NC	I/O	I/O	I/O	JP3.140
W11	NC	I/O	I/O	I/O	JP3.141
W22	NC	I/O	I/O	I/O	JP1.167
W23	NC	I/O	I/O	I/O	JP1.166

Tab. 4 Not Compatible Pins in All Family

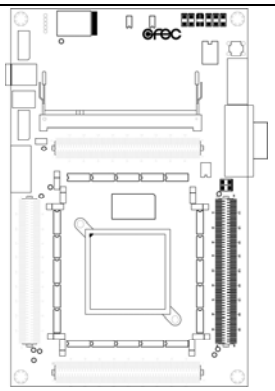
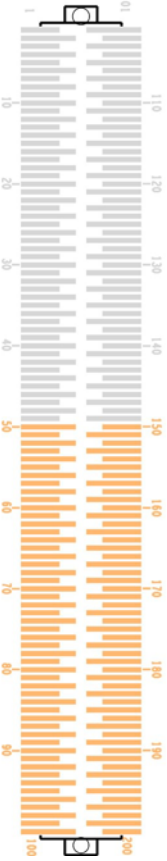
If there is any user I/O unused, we recommend to suspended joint them-unused pin to ground should be set in Quartus II- and the dedicate input should be pull high or pull low through a resistance.

2.5.1. JP1 & JP5

	Bank 2		Stratix II	Stratix II	
		1	GND	GND	101
		2	D32	F30	102
		3	D31	F29	103
		4	D30	G28	104
		5	D29	G27	105
		6	E32	H28	106
		7	E31	H27	107
		8	E30	J27	108
		9	E29	J26	109
		10	F32	K27	110
		11	F31	K26	111
		12	G32	K25	112
		13	G31	K24	113
		14	G30	L28	114
		15	G29	L27	115
		16	H32	L26	116
		17	H31	L25	117
		18	H30	L24	118
		19	H29	L23	119
		20	J32	M27	120
		21	J31	M26	121
		22	J30	M25	122
		23	J29	M24	123
		24	K32	M23	124
		25	K31	M22	125
		26	K30	N27	126
		27	K29	N26	127
		28	L32	N25	128
		29	L31	N24	129
		30	L30	N23	130
		31	L29	N22	131
		32	M32	P29	132
		33	M31	P28	133
		34	M30	P27	134
		35	M29	P26	135
		36	N31	P25	136
		37	N30	P24	137
		38	N29	P23	138
		39	N28	P22	139
		40	P32	R29	140
		41	P31	R28	141
		42	R31	R27	142
		43	R30	R26	143
		44	T32	R25	144
		45	T31	R24	145
		46	T30	R23	146
		47	T29	R22	147

		48	T28	T23	148
		49	T27	T22	149
		50	Reserve	GND	150

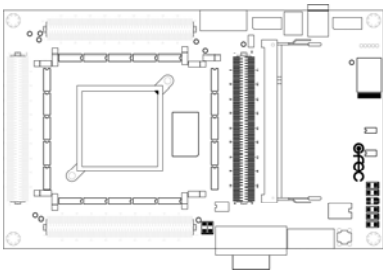
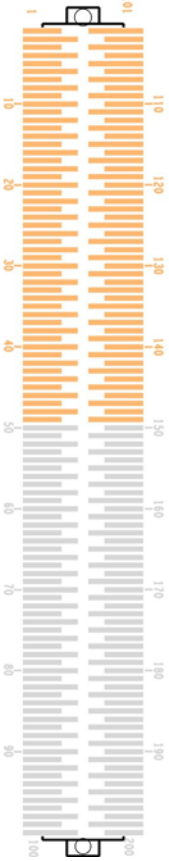
Tab. 5 JP1 & JP5 (I)

	Bank 1		Stratix II	Stratix II	
		51	Reserve	GND	151
		52	U32	U28	152
		53	U31	U27	153
		54	U30	U23	154
		55	U29	U22	155
		56	V31	V29	156
		57	V30	V28	157
		58	W32	V24	158
		59	W31	V23	159
		60	Y31	W29	160
		61	Y30	W28	161
		62	Y29	W27	162
		63	Y28	W26	163
		64	AA32	W25	164
		65	AA31	W24	165
		66	AA30	W23	166
		67	AA29	W22	167
		68	AB32	Y27	168
		69	AB31	Y26	169
		70	AB30	Y25	170
		71	AB29	Y24	171
		72	AC32	Y23	172
		73	AC31	Y22	173
		74	AC30	AA27	174
		75	AC29	AA26	175
		76	AD32	AA25	176
		77	AD31	AA24	177
		78	AD30	AA23	178
		79	AD29	AA22	179
		80	AE32	AB28	180
		81	AE31	AB27	181
		82	AE30	AB26	182
		83	AE29	AB25	183
		84	AF32	AB24	184
		85	AF31	AB23	185
		86	AF30	AC27	186
		87	AF29	AC26	187
		88	AG32	AC25	188
		89	AG31	AC24	189
		90	AG30	AD27	190
		91	AG29	AD26	191
		92	AH32	AD25	192
		93	AH31	AD24	193
		94	AH30	AE28	194
		95	AH29	AE27	195
		96	AJ32	AE26	196
		97	AJ31	AE25	197
		98	AJ30	AF28	198

		99	AJ29	AF27	199
		100	GND	GND	200

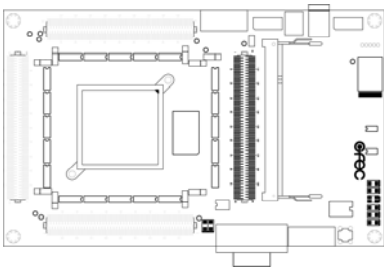
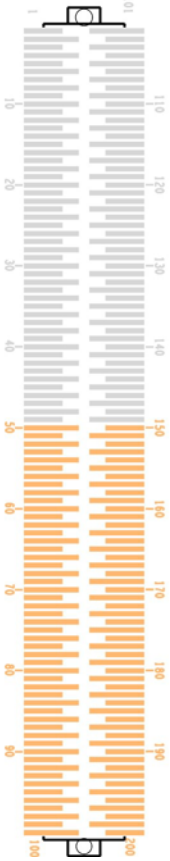
Tab. 6 JP1 & JP5 (II)

2.5.2. JP2 & JP6

	Bank 4		Stratix II	Stratix II	
		1	GND	GND	101
		2	TDO	GND	102
		3	A4	A9	103
		4	B4	B9	104
		5	C4	C9	105
		6	A5	E9	106
		7	B5	F9	107
		8	C5	C8	108
		9	D5	D8	109
		10	E5	E8	110
		11	A6	F8	111
		12	B6	A10	112
		13	C6	B10	113
		14	D6	C10	114
		15	E6	D10	115
		16	A7	F10	116
		17	B7	A11	117
		18	C7	B11	118
		19	D7	C11	119
		20	E7	D11	120
		21	A8	E11	121
		22	B8	F11	122
		23	A12	H9	123
		24	B12	G10	124
		25	C12	G11	125
		26	D12	H11	126
		27	F12	J11	127
		28	B13	K11	128
		29	C13	G12	129
		30	D13	H12	130
		31	E13	J12	131
		32	F13	K12	132
		33	G13	L12	133
		34	A14	H13	134
		35	B14	J13	135
		36	D14	K13	136
		37	E14	L13	137
		38	F14	G14	138
		39	F15	H14	139
		40	B15	J14	140
		41	C15	K14	141
		42	D15	L14	142
		43	E15	J15	143
		44	A16	K15	144
		45	B16	L15	145
		46	C16	K16	146
		47	D16	L16	147

		48	E16	K17	148
		49	F16	L17	149
		50	Reserve	GND	150

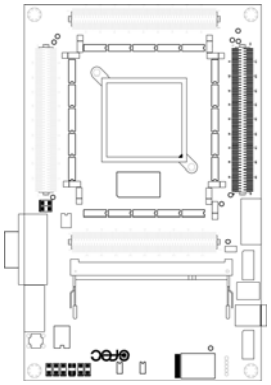
Tab. 7 JP2 & JP6 (I)

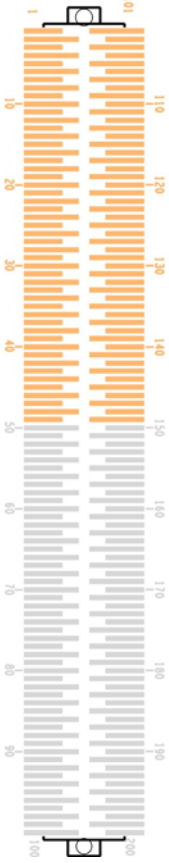
	Bank 3		Stratix II	Stratix II	
		51	Reserve	GND	151
		52	GND	Reserve	152
		53	GND	Reserve	153
		54	A17	NC	154
		55	B17	E17	155
		56	C17	F18	156
		57	D17	K18	157
		58	B18	L18	158
		59	C18	F19	159
		60	D18	J19	160
		61	E18	K19	161
		62	A19	L19	162
		63	B19	G20	163
		64	E19	H20	164
		65	D19	J20	165
		66	F20	K20	166
		67	E20	L20	167
		68	D20	G21	168
		69	C20	H21	169
		70	B20	J21	170
		71	F21	K21	171
		72	D21	L21	172
		73	C21	G22	173
		74	B21	H22	174
		75	A21	J22	175
		76	F22	K22	176
		77	E22	L22	177
		78	D22	G23	178
		79	C22	H23	179
		80	B22	J23	180
		81	A22	G24	181
		82	A26	H24	182
		83	B26	A23	183
		84	C26	B23	184
		85	D26	C23	185
		86	E26	D23	186
		87	A27	F23	187
		88	B27	A24	188
		89	C27	B24	189
		90	D27	C24	190
		91	E27	E24	191
		92	E28	F24	192
		93	D28	A25	193
		94	A28	B25	194
		95	B28	C25	195
		96	C28	D25	196

		97	A29	E25	197
		98	B29	F25	198
		99	C29	G25	199
		100	GND	GND	200

Tab. 8 JP2 & JP6 (II)

2.5.3. JP3 & JP7

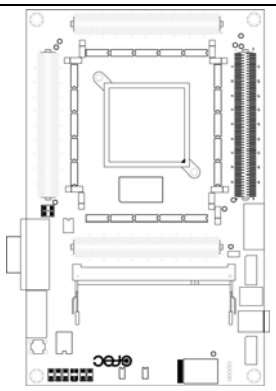
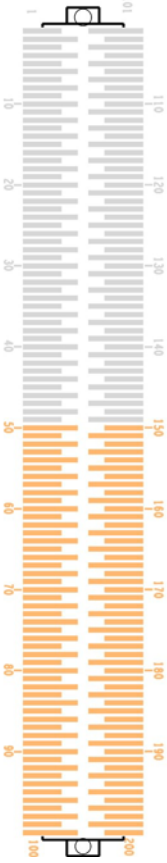




Bank 6		Stratix II	Stratix II	
	1	GND	GND	101
	2	AJ1	AG3	102
	3	AJ2	AG4	103
	4	AJ3	AF5	104
	5	AJ4	AF6	105
	6	AH1	AE5	106
	7	AH2	AE6	107
	8	AH3	AD6	108
	9	AH4	AD7	109
	10	AG1	AD8	110
	11	AG2	AD9	111
	12	AF1	AC6	112
	13	AF2	AC7	113
	14	AF3	AC8	114
	15	AF4	AC9	115
	16	AE1	AB5	116
	17	AE2	AB6	117
	18	AE3	AB7	118
	19	AE4	AB8	119
	20	AD1	AB9	120
	21	AD2	AB10	121
	22	AD3	AA6	122
	23	AD4	AA7	123
	24	AC1	AA8	124
	25	AC2	AA9	125
	26	AC3	AA10	126
	27	AC4	AA11	127
	28	AB1	Y6	128
	29	AB2	Y7	129
	30	AB3	Y8	130
	31	AB4	Y9	131
	32	AA1	Y10	132
	33	AA2	Y11	133
	34	AA3	W4	134
	35	AA4	W5	135
	36	Y2	W6	136
	37	Y3	W7	137
	38	Y4	W8	138
	39	Y5	W9	139
	40	W1	W10	140
	41	W2	W11	141
	42	V2	V4	142
	43	V3	V5	143
	44	U1	V6	144
	45	U2	V7	145

		46	U3	V9	146
		47	U4	V10	147
		48	U5	U10	148
		49	U6	U11	149
		50	Reserve	GND	150

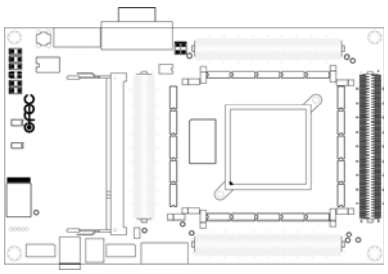
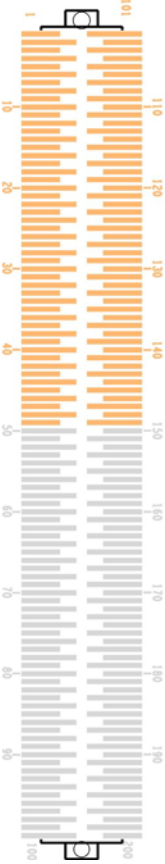
Tab. 9 JP3 & JP7(I)

	Bank 5		Stratix II	Stratix II	
		51	Reserve	GND	151
		52	T1	T5	152
		53	T2	T6	153
		54	T3	T10	154
		55	T4	T11	155
		56	R2	R4	156
		57	R3	R5	157
		58	P1	R6	158
		59	P2	R7	159
		60	N2	R10	160
		61	N3	R11	161
		62	N4	P4	162
		63	N5	P5	163
		64	M1	P6	164
		65	M2	P7	165
		66	M3	P8	166
		67	M4	P9	167
		68	L1	P10	168
		69	L2	P11	169
		70	L3	N6	170
		71	L4	N7	171
		72	K1	N8	172
		73	K2	N9	173
		74	K3	N10	174
		75	K4	N11	175
		76	J1	M6	176
		77	J2	M7	177
		78	J3	M8	178
		79	J4	M9	179
		80	H1	M10	180
		81	H2	M11	181
		82	H3	L5	182
		83	H4	L6	183
		84	G1	L7	184
		85	G2	L8	185
		86	G3	L9	186
		87	G4	L10	187
		88	F1	K6	188
		89	F2	K7	189
		90	F3	K8	190
		91	F4	K9	191
		92	E1	J6	192
		93	E2	J7	193
		94	E3	J8	194

		95	E4	J9	195
		96	D1	H5	196
		97	D2	H6	197
		98	D3	G5	198
		99	D4	G6	199
		100	GND	GND	200

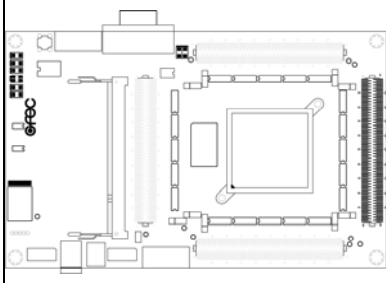
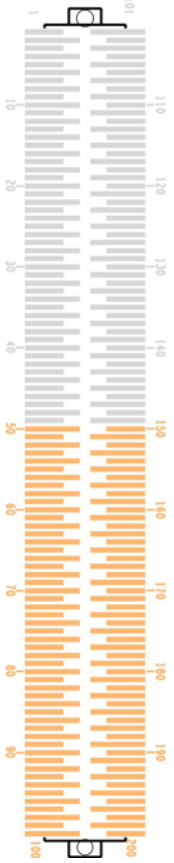
Tab. 10 JP3 & JP7 (II)

2.5.4. JP4 & JP8

	Bank 8		Stratix II	Stratix II	
		1	GND	GND	101
		2	AM29	Reserve	102
		3	AL29	AH28	103
		4	AK29	AH26	104
		5	AM28	AH25	105
		6	AL28	AG25	106
		7	AK28	AH24	107
		8	AJ28	AG24	108
		9	AM27	Reserve	109
		10	AL27	Reserve	110
		11	AK27	AG23	111
		12	AJ27	AF23	112
		13	AM26	AE23	113
		14	AL26	AD23	114
		15	AK26	AH22	115
		16	AJ26	AG22	116
		17	AM25	AF22	117
		18	AL25	AE22	118
		19	AK25	AC22	119
		20	AJ25	AD22	120
		21	AM24	AG21	121
		22	AL24	AF21	122
		23	AK24	AE21	123
		24	AM23	AD21	124
		25	AL23	AC21	125
		26	AK23	AB21	126
		27	AJ23	AH20	127
		28	AM22	AG20	128
		29	AL22	AF20	129
		30	AK22	AE20	130
		31	AJ22	AD20	131
		32	AM21	AC20	132
		33	AL21	AB20	133
		34	AK21	AH19	134
		35	AJ21	AG19	135
		36	AL20	AF19	136
		37	AK20	AE19	137
		38	AJ20	AD19	138
		39	AJ19	AC19	139
		40	AM19	AB19	140
		41	AL19	AG18	141
		42	AL18	AD18	142
		43	AK18	AC18	143

		44	AJ18	AB18	144
		45	AH18	AH17	145
		46	AM17	AG17	146
		47	AL17	AC17	147
		48	AK17	AB17	148
		49	AJ17	GND	149
		50	Reserve	GND	150

Tab. 11 JP4 & JP8 (I)

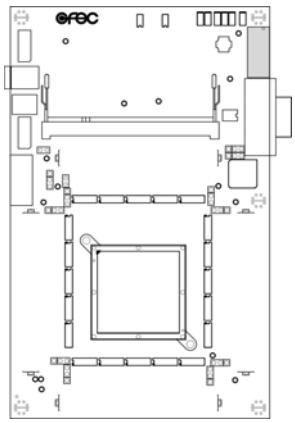
	Bank 7		Stratix II	Stratix II	
		51	Reserve	GND	151
		52	AM16	GND	152
		53	AL16	AC16	153
		54	AK16	AB16	154
		55	AJ16	AC15	155
		56	AH16	AB15	156
		57	AG16	AF14	157
		58	AL15	AE14	158
		59	AK15	AD14	159
		60	AJ15	AC14	160
		61	AH15	AB14	161
		62	AM14	AG15	162
		63	AL14	AH14	163
		64	AJ14	AG14	164
		65	AL13	AH13	165
		66	AK13	AG13	166
		67	AJ13	AF13	167
		68	AM12	AE13	168
		69	AL12	AD13	169
		70	AK12	AC13	170
		71	AJ12	AB13	171
		72	AM11	AG12	172
		73	AL11	AF12	173
		74	AK11	AE12	174
		75	AM10	AD12	175
		76	AL10	AC12	176
		77	AK10	AB12	177
		78	AM9	AD11	178
		79	AL9	AC11	179
		80	AK9	AB11	180
		81	AM8	AD10	181
		82	AL8	AJ11	182
		83	AK8	AH11	183
		84	AJ8	AG11	184
		85	AM7	AF11	185
		86	AL7	AE11	186
		87	AK7	AJ10	187
		88	AJ7	AG10	188
		89	AM6	AF10	189
		90	AL6	AE10	190
		91	AK6	AH9	191
		92	AJ6	AG9	192

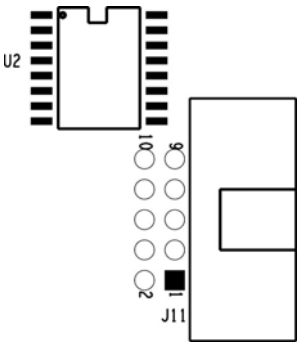
		93	AM5	AE9	193
		94	Al5	AH8	194
		95	AK5	AG8	195
		96	AJ5	AF8	196
		97	AM4	AH7	197
		98	AL4	AH6	198
		99	AK4	AH5	199
		100	GND	GND	200

Tab. 12 JP4 & JP8 (II)

2.6. Specification of Configuration EPROM

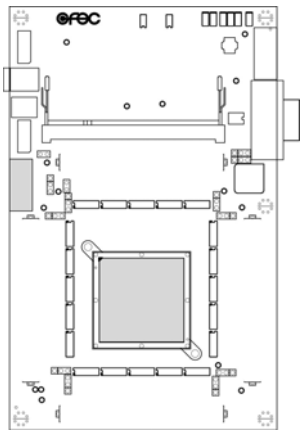
Altera FPGA can be burned in many planning way. The development board has been attached Configuration Device EPCS64 or EPCS16(configured according to chosen capacity of FPGA) before shipping. And AS connection port is reserved on the board, which can be used for Configuration Device-EPCS16SI16N & EPCS64SI64N by attached GFEC USB Blaster or Byte Blaster II Download Cable. The detailed use method of ISP refers to 3.3.2, and these should be operated step by step.

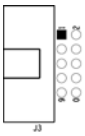


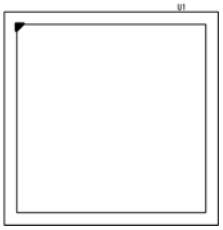


2.7. JTAG

The development board provides one JTAG connector, which is used in the early stage when RTL code has not finished and burning programme has to be changed frequently. It can reduce the burning time and burning times when using configuration device.



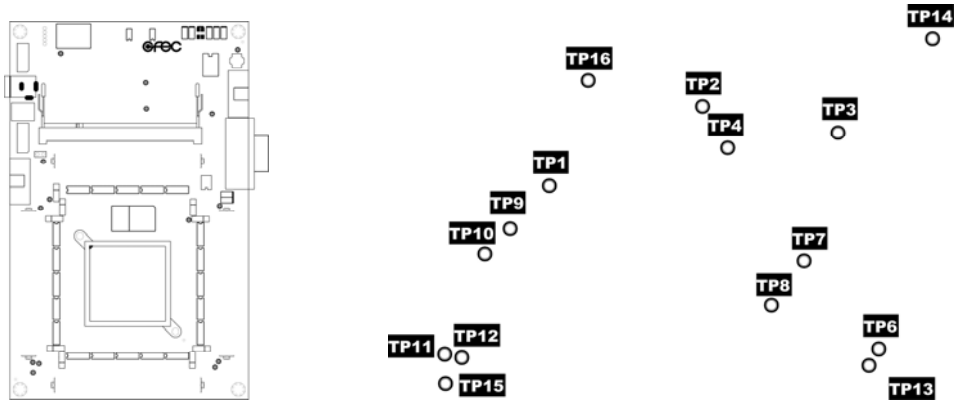




2.8. Test Pin

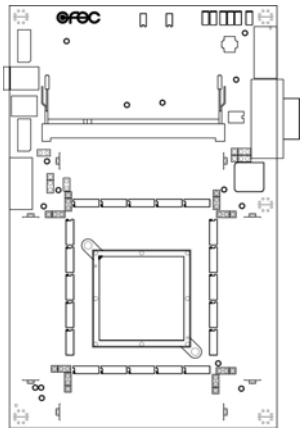
The development board offers 16 test pins in total, which are used to indicate the system status during validation.

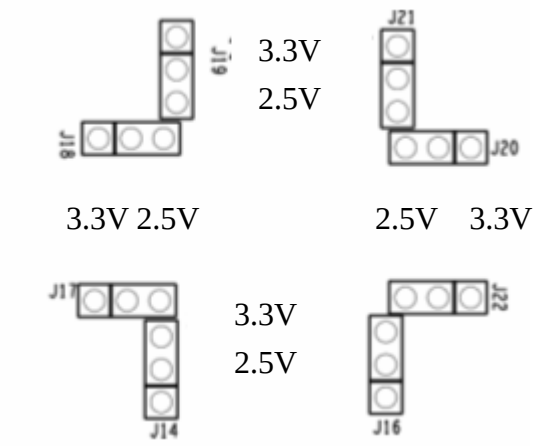
Test Pin Name	Power
TP1	GND
TP2	4.3 V
TP3	3.3 V
TP4	2.5 V
TP6	Bank 1 VCCIO
TP7	Bank 2 VCCIO
TP8	Bank 3 VCCIO
TP9	Bank 4 VCCIO
TP10	Bank 5 VCCIO
TP11	Bank 6 VCCIO
TP12	Bank 7 VCCIO
TP13	Bank 8 VCCIO
TP14	GND
TP15	GND
TP16	GND
TP17	1.2 V



2.9. Jumper-Choosing Area

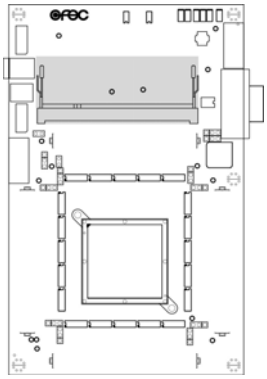
According to customer's requirement, voltage of every I/O bank of the development board can be adjusted as 3.3V and 2.5V.

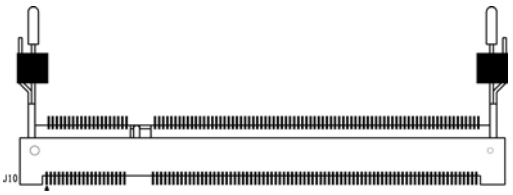




2.10. DDR So-DIMM

The development board offers one DDR So-DIMM pin, which is for designs needing DDR SDRAM. The function is pre-set as Disabled. Customers have to process impedance matching resistance of 16P8R 50 Ohm by themselves when this function is needed.



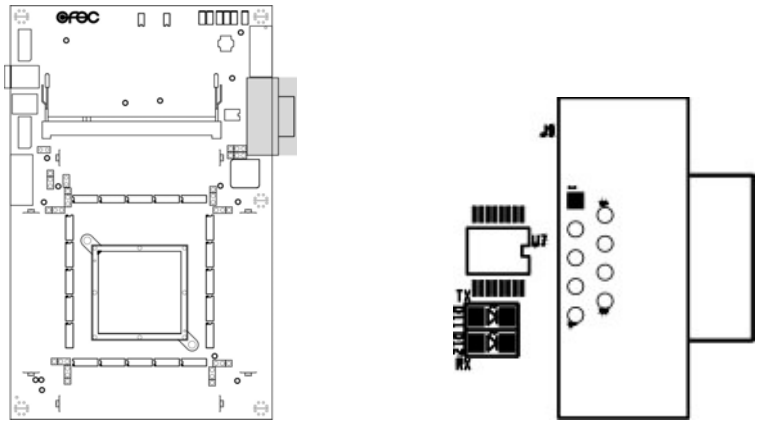


2.11. UART

The development board offers one RS-232 connector to be used when necessary. RTS and CTS in the second group only can be used for FPGA higher than EP2S90F1020.

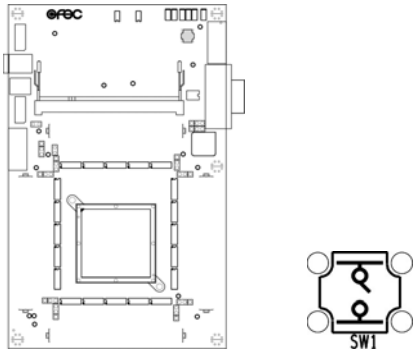
Pin Name	Bank	Location	Board Location
UART TXD	B2	F30	J1.4
UART RXD	B2	F29	J1.5
UART RTS	B2	G28	J1.104
UART CTS	B2	G27	J1.105

Tab. 13 UART in GFEC Stratix II Development Board



2.12. Re-Configuration

The board offers one Push Button Switch (SW1), which provides re-download from Serial Configuration Device to FPGA.



2.13. Usage of Clock Signal

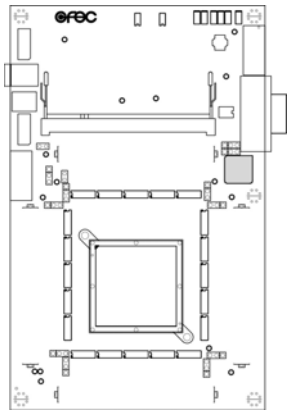
The development board offers two ways to lead in clock signal:

- Extension I/O Connector
- Oscillator Socket (Half size)

Quartz oscillator is pre-set as the input of clock signal, and input clock signal to global clock 15, details as follow:

Type	Bank	Global Clock Name	Location	Board Location
Full Size Osillator Socket	B3	GCLK 15	E16	JP2.48

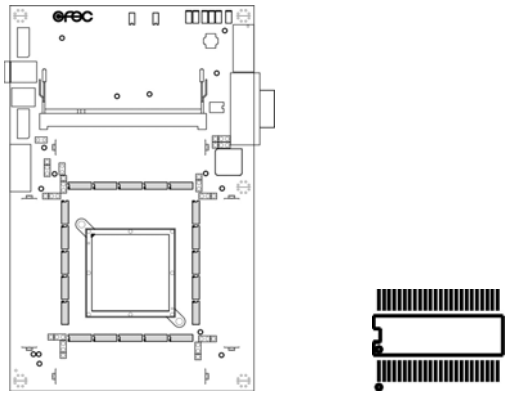
Tab. 14 Global Clock in GFEC Stratix II Development Board



Half Size Oscillator Socket

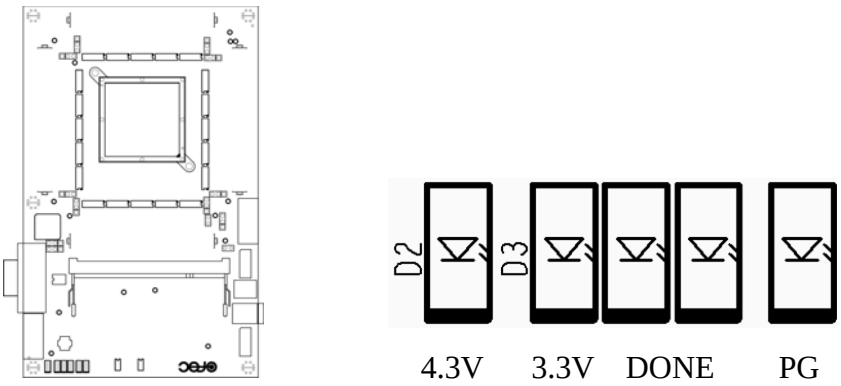
2.14. Electric Specification and Characteristics of I/O Follow Through Switch

In the development board, all Stratix II FPGA I/Os reach JP1~JP8 through Follow Through Switch; Per buffer offers 20 channels. Each buffer only offers max. 0.5 Watt power although each channel can offer max. 120mA. Therefore, the power is dispersed in different piece of buffer when more than one group of high current is needed. Details about Follow Through Switch refer to the appendix.



2.15. System Status Indicators

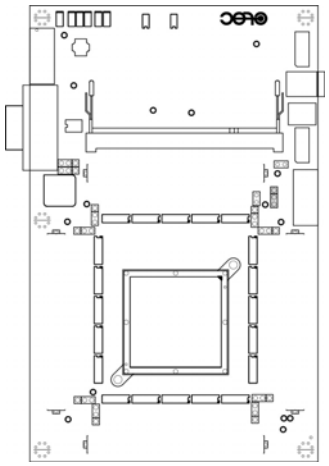
Five LEDs are offered on the development board – System Power Good, Done(It means the configuration is successful if the green light becomes light or the configuration is failed if the red light becomes light),4.3V Power Good 3.3V Power Good



2.16. Stacking

If the FPGA Gate Count offered by the development board is not enough, you can extend it by stacking up and down. The only thing should be paid attention is that there should not be any confliction between pins definition, so as to avoid damaging Follow Through Switch.

The development board offers TAG chain. Through JTAG chain , FPGA can be joint up in series with J26.



3. Information About Software

3.1. QuartusII Version Support

QuartusII with version no lower than 4.0 supports Stratix II Device Family. You will receive optical disk for upgrading from Altera itself when your software is within warranty period, you can also apply for trail software from GFEC.

Platform & Hardware	OS	OS Service Packs or Patches
PC **System requirements:** **800 Mbytes disk space** **256 Mbytes RAM** *(1)*	Windows XP	None
	Windows NT 4.0	Service Pack 3 or greater
	Windows 2000	None
	RedHat Linux 8.0	None
	RedHat Linux 7.3	None
	RedHat Enterprise Linux 3	None
SUN **System requirements:** **1.1 Gbytes disk space** **256 Mbytes RAM** *(1)*	Solaris 9	None
	Solaris 8	*(2)*
HP **System requirements:** **925 Mbytes disk space** **256 Mbytes RAM** *(1)*	HP-UX 11.0	*(2)*

Tab. 15 contains details about Quartus® II software version 4.2 operating system (OS) support.

Stratix II Device Availability POF

	Software Support		
	Preliminary Timing Models	POF Support	Final Timing Models
EP2S15	V4.0	V4.2 SP1	v5.0
EP2S30	V4.0	V4.2	v5.0
EP2S60	V4.0	V4.1 SP1	v5.0
EP2S90	V4.0	V4.2 SP1	v5.0
EP2S130	V4.0	V4.2	v5.0
EP2S180	V4.0	V4.2 SP1	v5.0

Tab. 16 Quartus II Support Stratix II Timing Model & POF

3.2. Version Support from Cooperation Manufacturer

Product		Version
Vendor	Product	
Mentor Graphics	Precision	2003c
Synplicity	Synplify	7.5

Tab. 17 3rd Support Stratix II device family

3.3. Software Operation

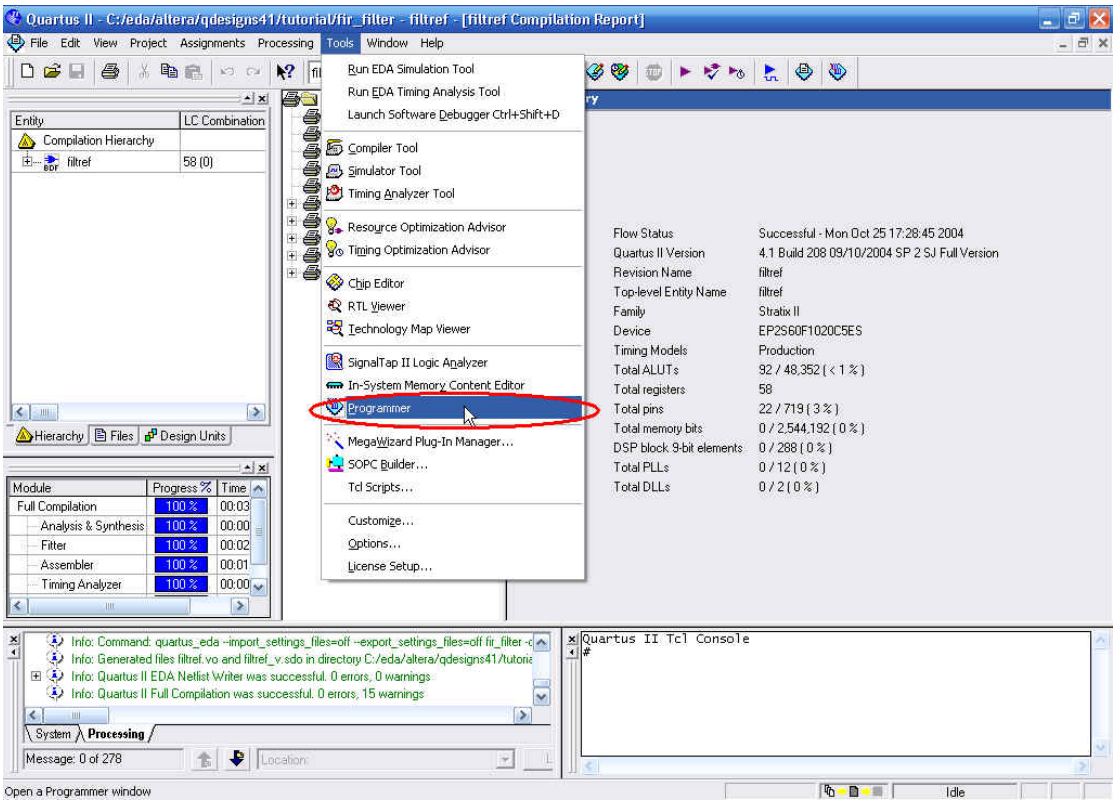
Since FPGA is fabricated on the basis of SRAM fab, the development board offers two mode - JTAG(*.SOF) and AS(*.POF)- to plan FPGA. JTAG mode is mainly used to plan FPGA and AS mode is mainly used to burn Serial EPROM. The following explains the burning operation step by step.

If your purpose is only to burn FPGA or EPROM in lab and not to compile it, it's not necessary for you to install the wholeQuartus II. It's enough to install Quartus II Programmer Only. This programme is about 20~30MB, it can save some space on the hardware and doesn't occupy system resource. You can operate them in the same way. This programme can be download from Altera website, or look it up in the installation CD supplied by GFEC.

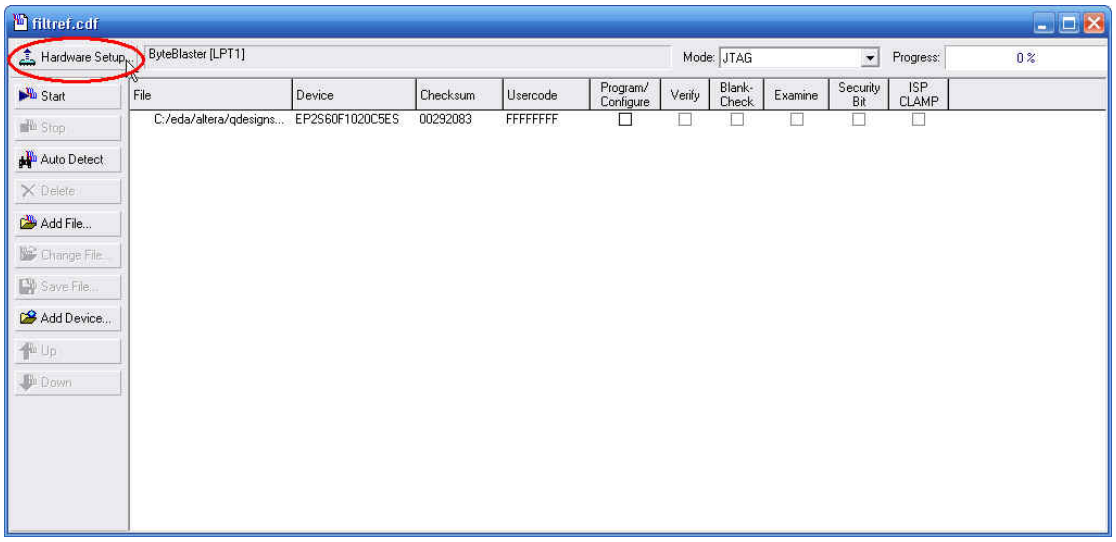
3.3.1. JTAG

Presently, JTAG is mainly used to planAltera Stratix II FPGA. Burning file SOF which is generated by Quartus II is necessary for the planning. In this mode, data will disappear when power is shut down. The operation should be repeated after enable the power of the board.

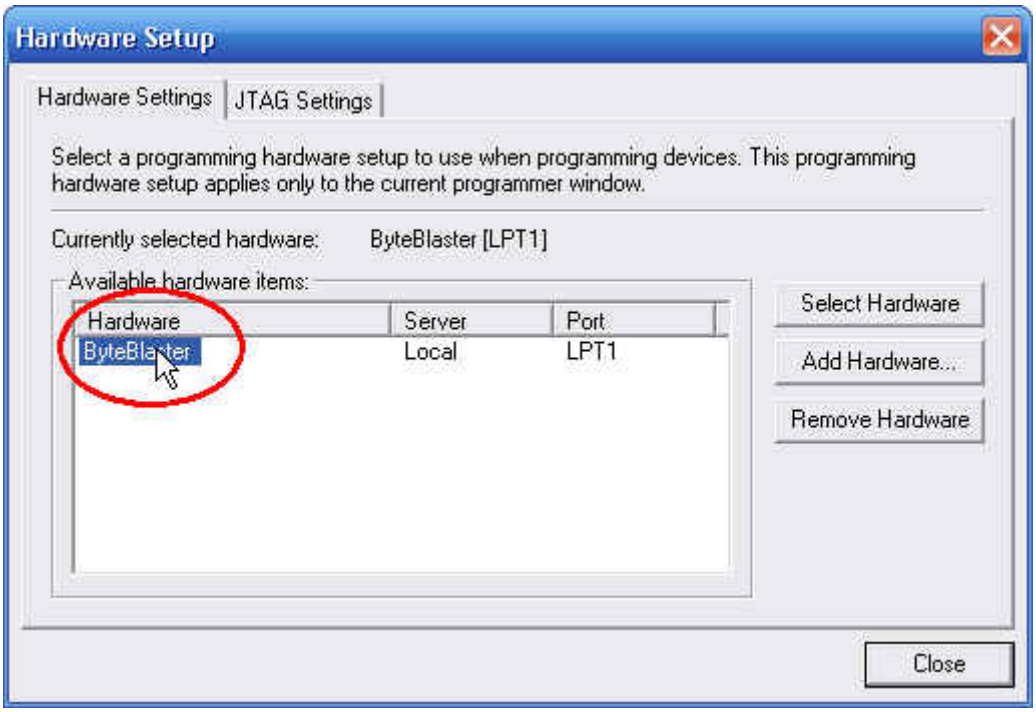
1. Execute: Quartus II → Tools → Programmer.



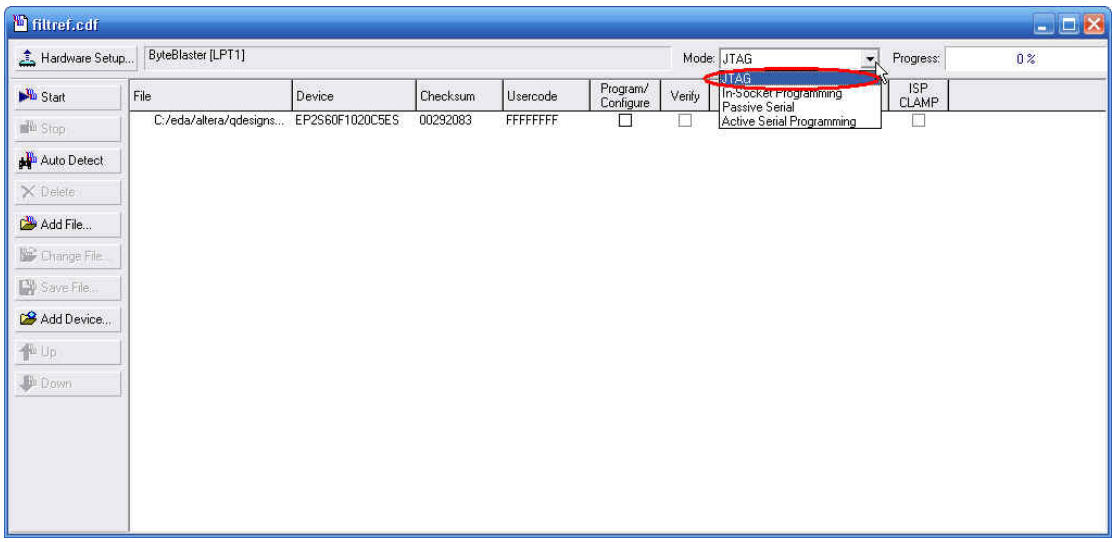
2. Setup hardware to be burned.



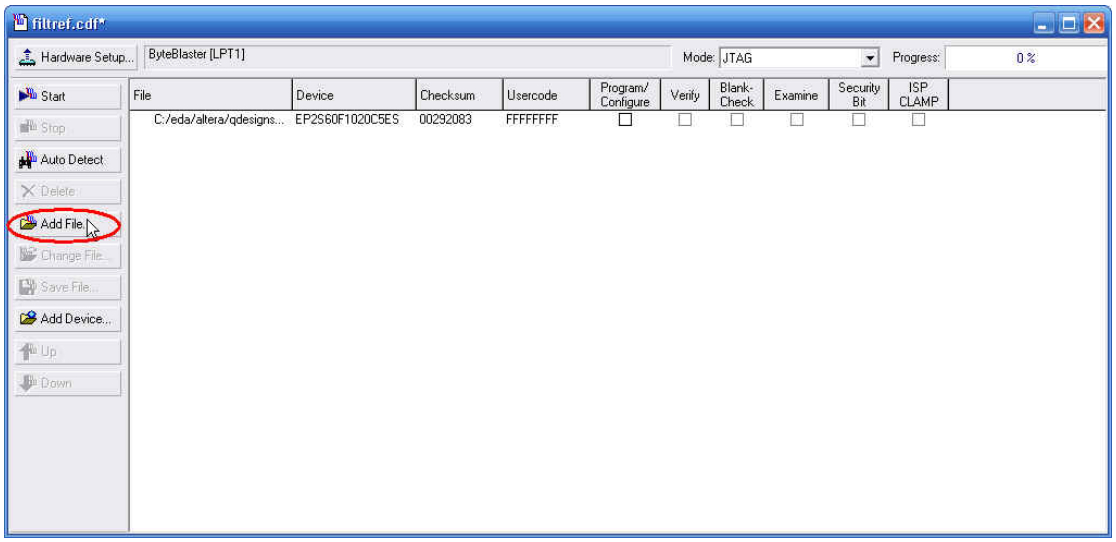
3. Choose the hardware used currently: Bytebalster II, Byteblaster MV or USB-Blaster.



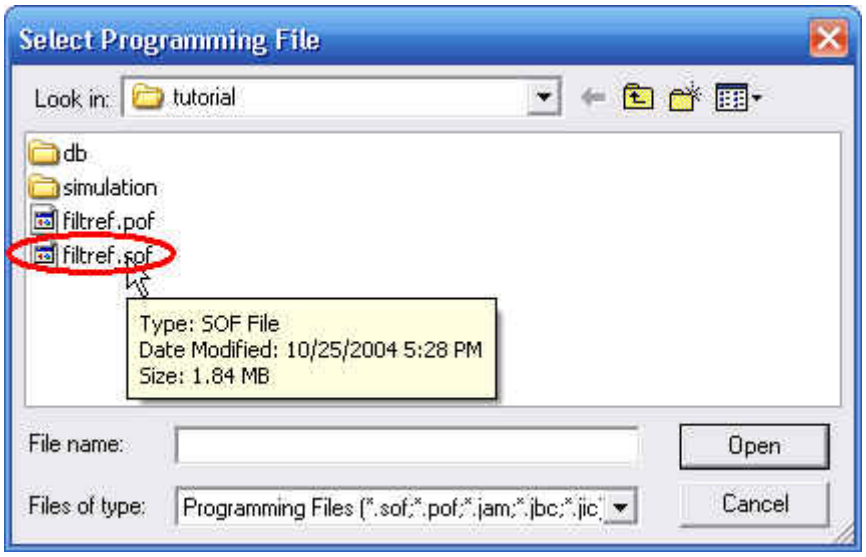
4. Choose JTAG mode.



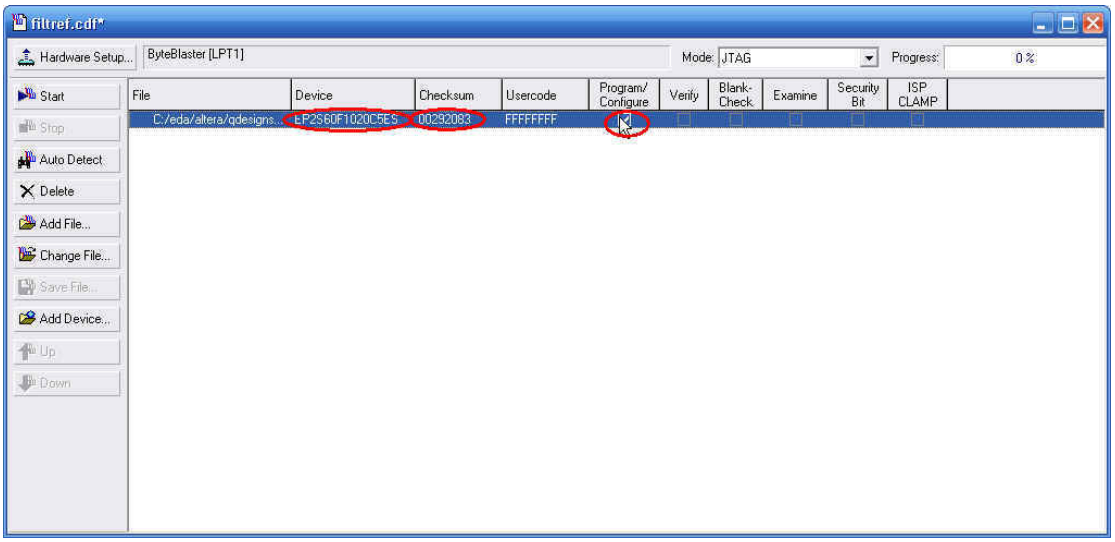
5. Add files in Add File.



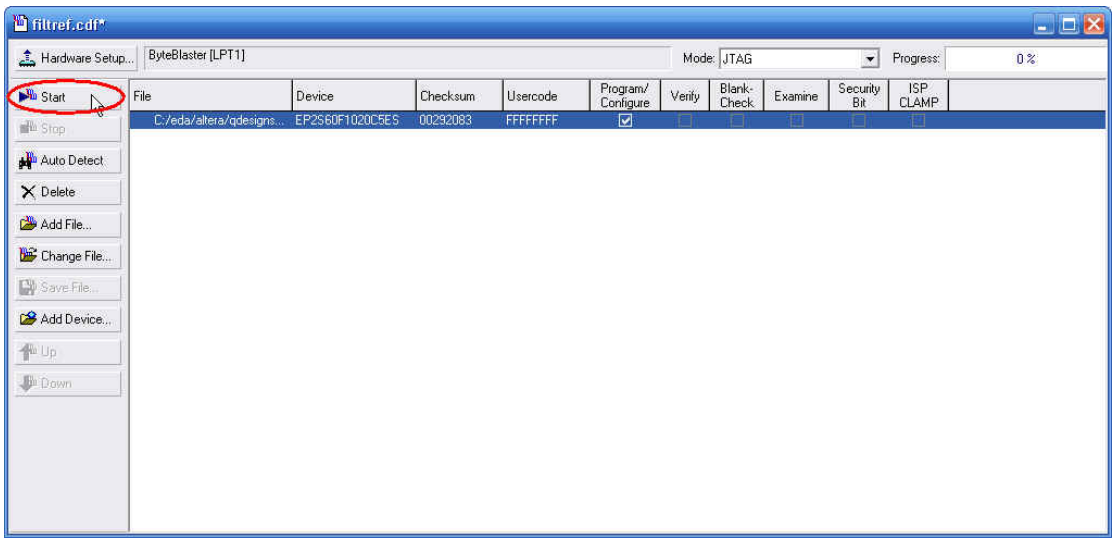
6. Choose the files to be burned (*.POF) .



7. Confirm Checksum and Device, and click Program/configure.



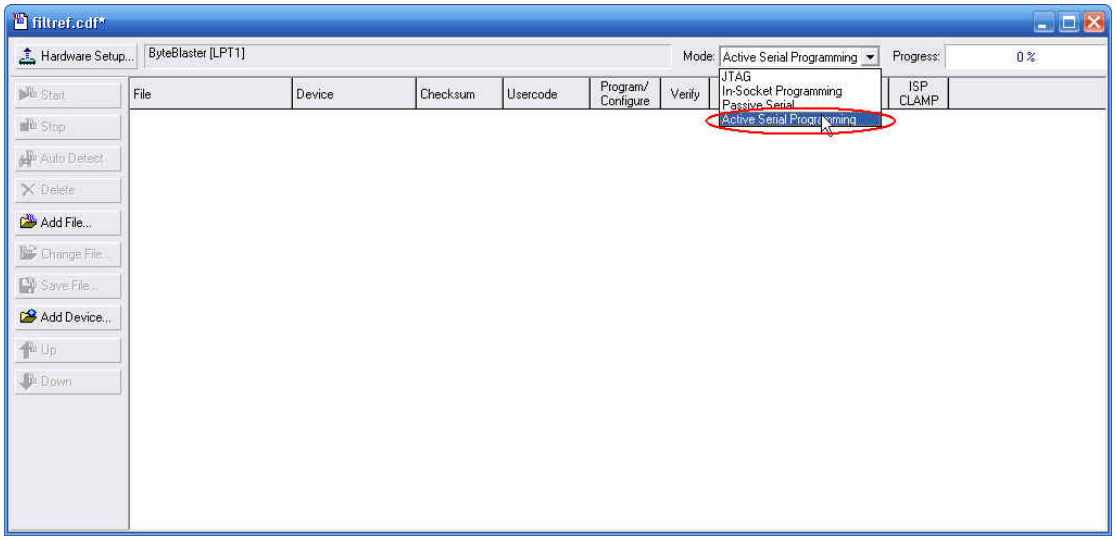
8. Start burning.



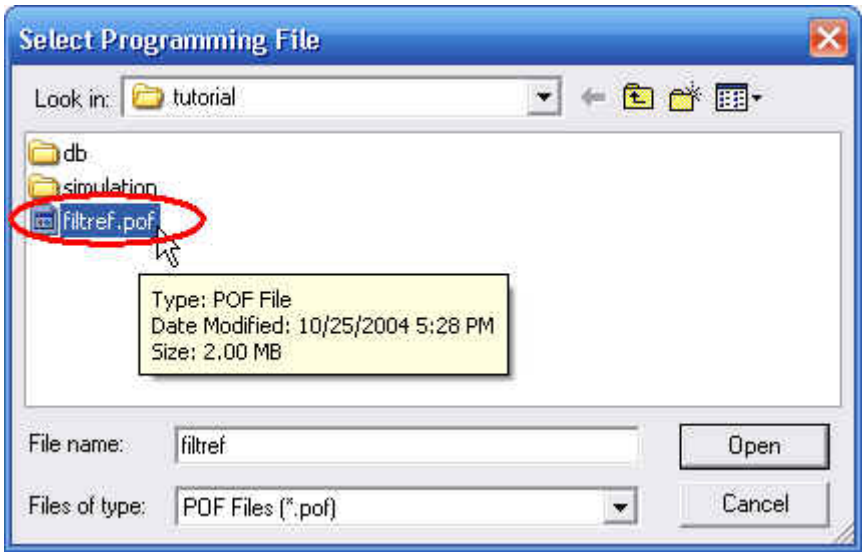
3.3.2. Active Serial Programming (AS)

If Serial Configuration Device (EPCS16SI16N 和 EPCS64SI16N) is burned in the mode of Active Serial Programming (AS) , once the burning is finished, Altera Stratix II Device Family will plan automatically each time the board power enabled.

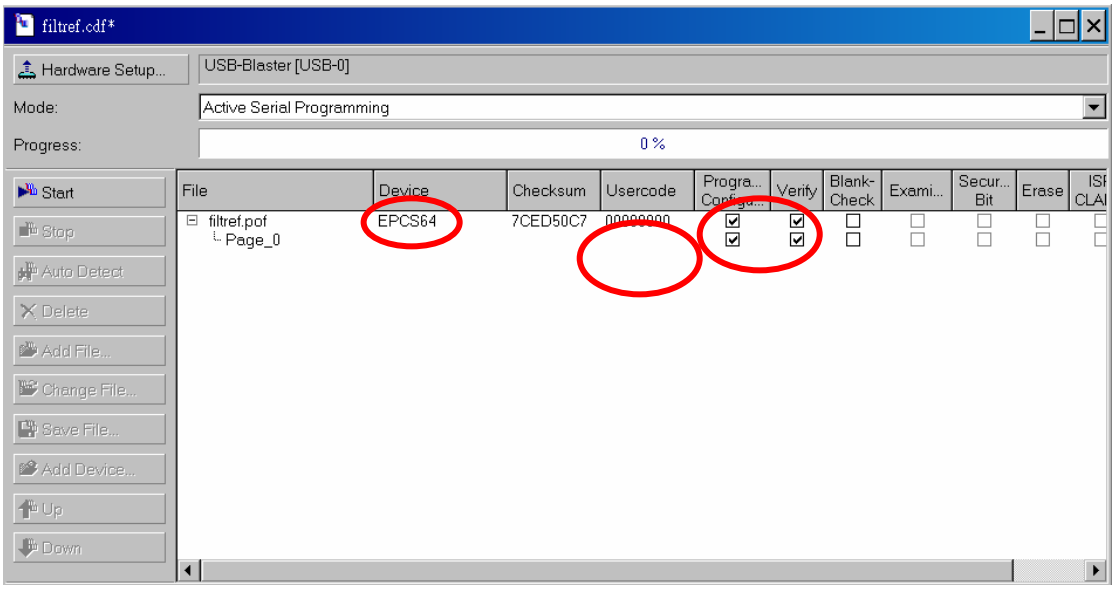
1. Choose Active Serial Programming Mode. If Hardware Setup is set as No Hardware, repeat Step 2 ~ Step 3 in 3.3.1 JTAG mode.



2. Choose files (*.POF) to be burned into Serial EPROM.



3. Confirm Device, Checksum and Program/Configure, and check them.



4. Choose Start to begin burning.

4. Appendix

4.1. Guide for Installing Byteblaster MV/II in Windows 2K/XP

During hardware setup, if no hardware can be found, the installation should be performed manually according to the following steps.

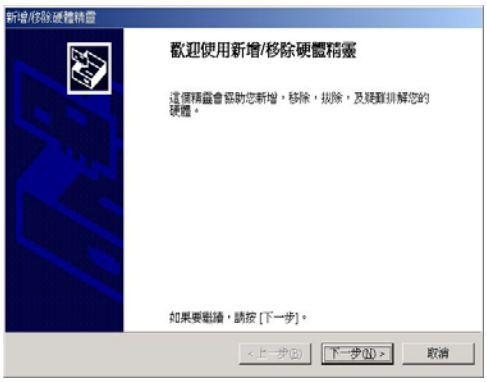
1. Support version :
   - Maxplus2 9.6 or later
   - Quartus 2000.03 or later

2. DRIVERS PATH :
   - -Maxplus2 <Maxplus2 install path >\Drivers\win2000\
     Default path=c:\maxplus2\drivers\win2000
   - -Quartus <Quartus install path>\Drivers\win2000
     Default path=c:\Quartus\drivers\win2000

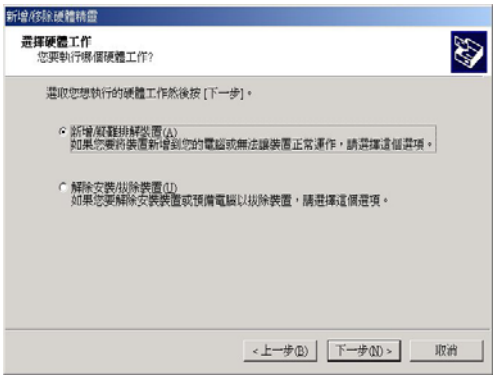
3. PROGRAMME INSTALLATION
   - Enter Control Panel

   - Select

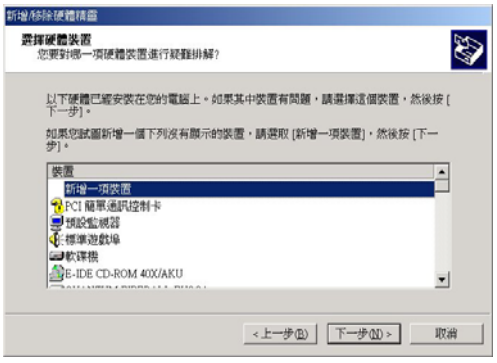
   - Choose Next



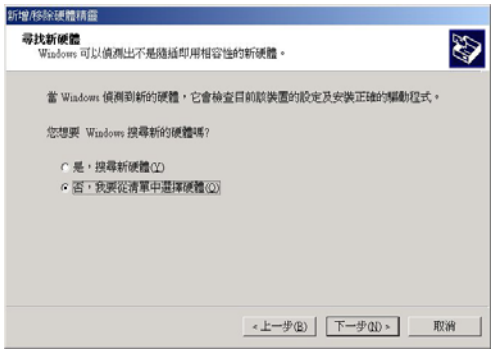
- Choose Next



- Choose Add a new hardware/software

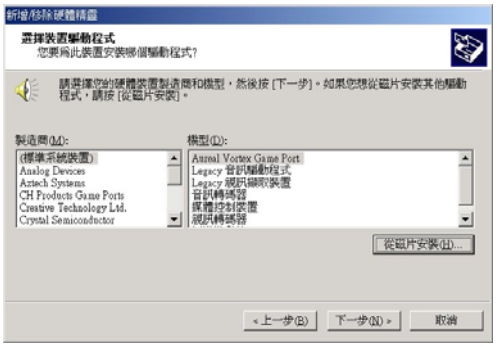


- Choose No, I want to choose hardware from list

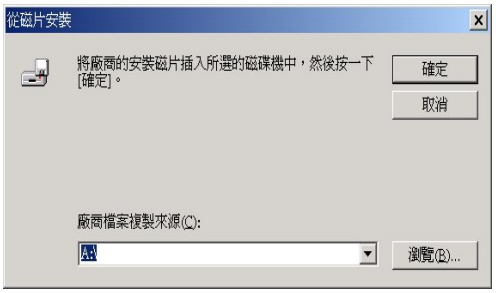


- Choose Sound effect, video and game controller

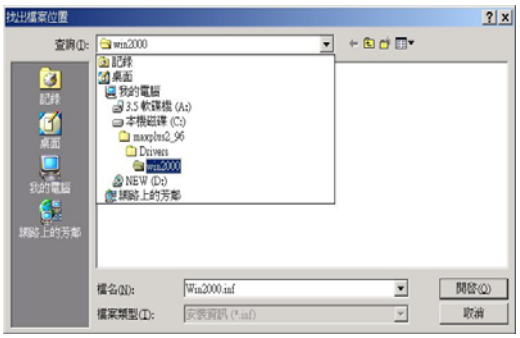
- Choose Installation from disk



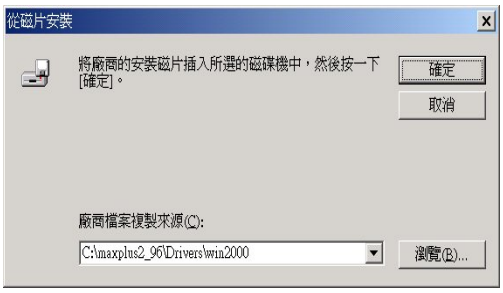
- Choose Browse



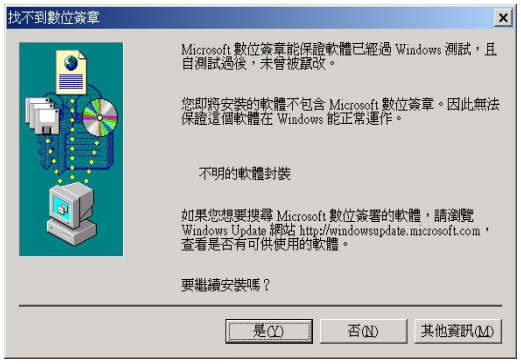
- Choose Open after finding files location



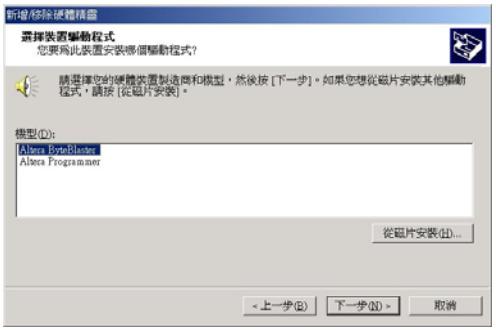
- Choose OK



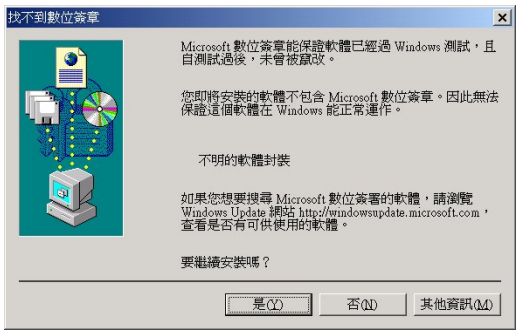
- Choose Yes



- Choose Altera Byteblaster

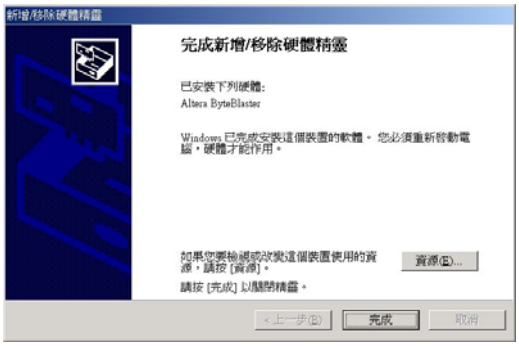


- Choose Yes

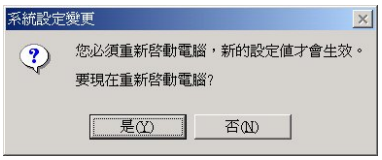


- Choose Next

- Choose Finish

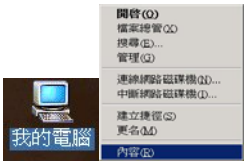


- Restart computer

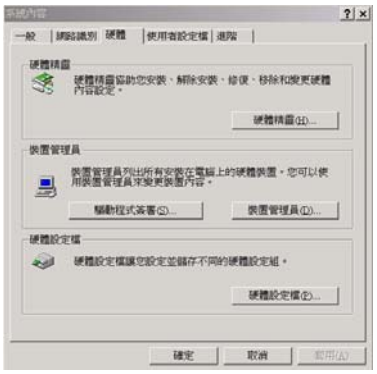


4. CONFIRM WHETHER THE INSTALLATION IS SUCCESSFUL

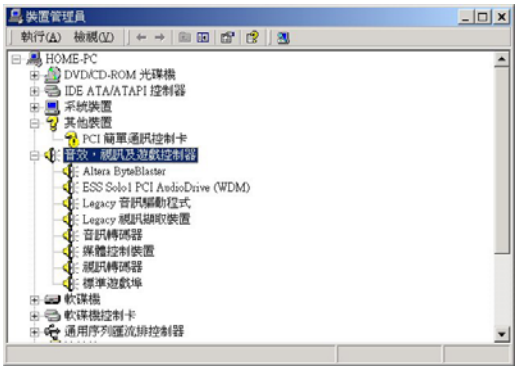
- Return to the desktop, choose My computer, then click the right key of mouse and choose Content.



- Choose Administrator under hardware



- Choose Sound effect, video and game controller



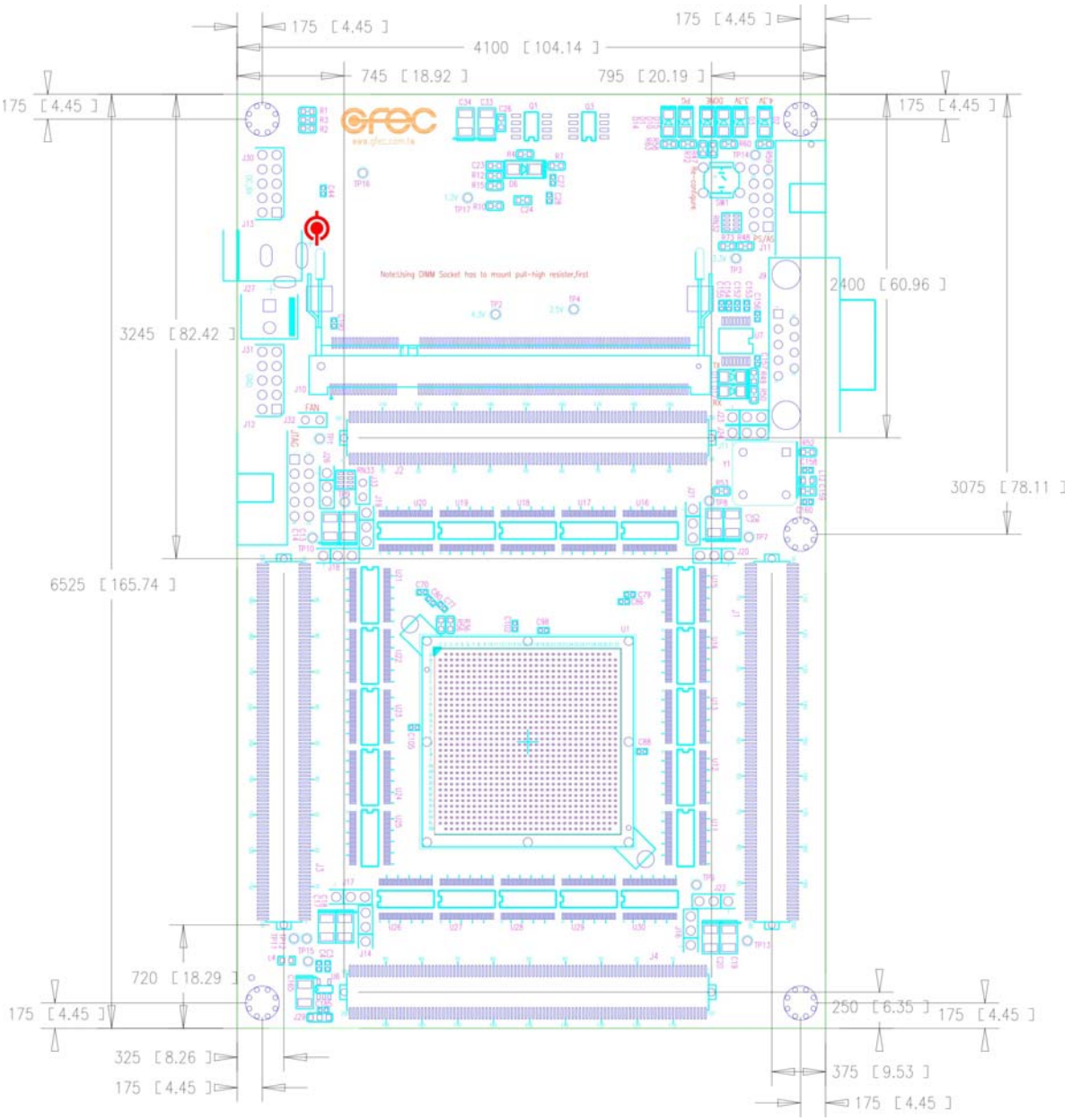
If Altera Byteblaster appears, it means that the installation has succeeded !!

4.2. Modify the Compatibility of Microsoft Window XP SP2

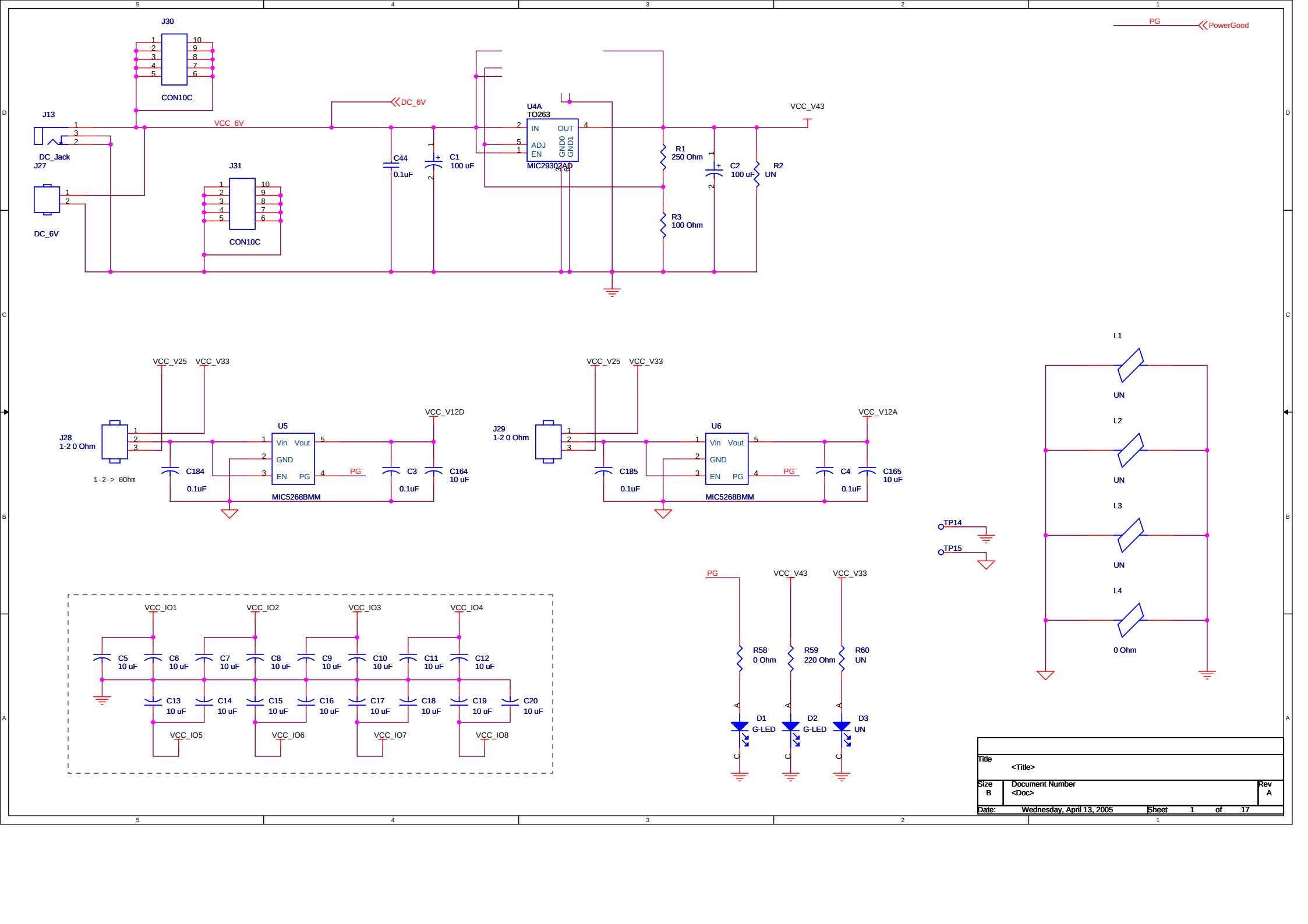
In Microsoft Window XP, if the user installs Quartus II firstly and then installs Windows XP SP2, he has to re-install Byteblaster driver, and then download programme onto the hardware. Do the re-installation as follow:

Cd quartus\drivers\i386
Bblpt.exe /r —removes the ByteBlaster driver
Bblpt /i —reinstalls the ByteBlaster driver
Net start ALTERABYTEBLASTER

4.3. Dimensional Drawing



4.4. Schematic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CON10C
J13
DC_Jack
J27
DC_6V
VCC_6V
J31
CON10C
DC_6V
C44
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C1
100 uF
U4A
TO263
IN
OUT
ADJ
EN
GND0
GND1
MIC29302AD
VCC_V43
R1
250 Ohm
C2
100 uF
R2
UN
R3
100 Ohm
PG
PowerGood
VCC_V25
VCC_V33
J28
1-2 0 Ohm
1-2-> 00hm
C184
0.1uF
U5
Vin
Vout
GND
EN
PG
MIC5268BMM
C3
0.1uF
C164
10 uF
VCC_V12D
J29
1-2 0 Ohm
C185
0.1uF
U6
C4
0.1uF
C165
10 uF
VCC_V12A
TP14
TP15
L1
UN
L2
UN
L3
UN
L4
0 Ohm
VCC_IO1
VCC_IO2
VCC_IO3
VCC_IO4
C5 10 uF
C6 10 uF
C7 10 uF
C8 10 uF
C9 10 uF
C10 10 uF
C11 10 uF
C12 10 uF
C13 10 uF
C14 10 uF
C15 10 uF
C16 10 uF
C17 10 uF
C18 10 uF
C19 10 uF
C20 10 uF
VCC_IO5
VCC_IO6
VCC_IO7
VCC_IO8
PG
VCC_V43
VCC_V33
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D2
G-LED
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Rev
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Date:
Wednesday, April 13, 2005
Sheet
1
of
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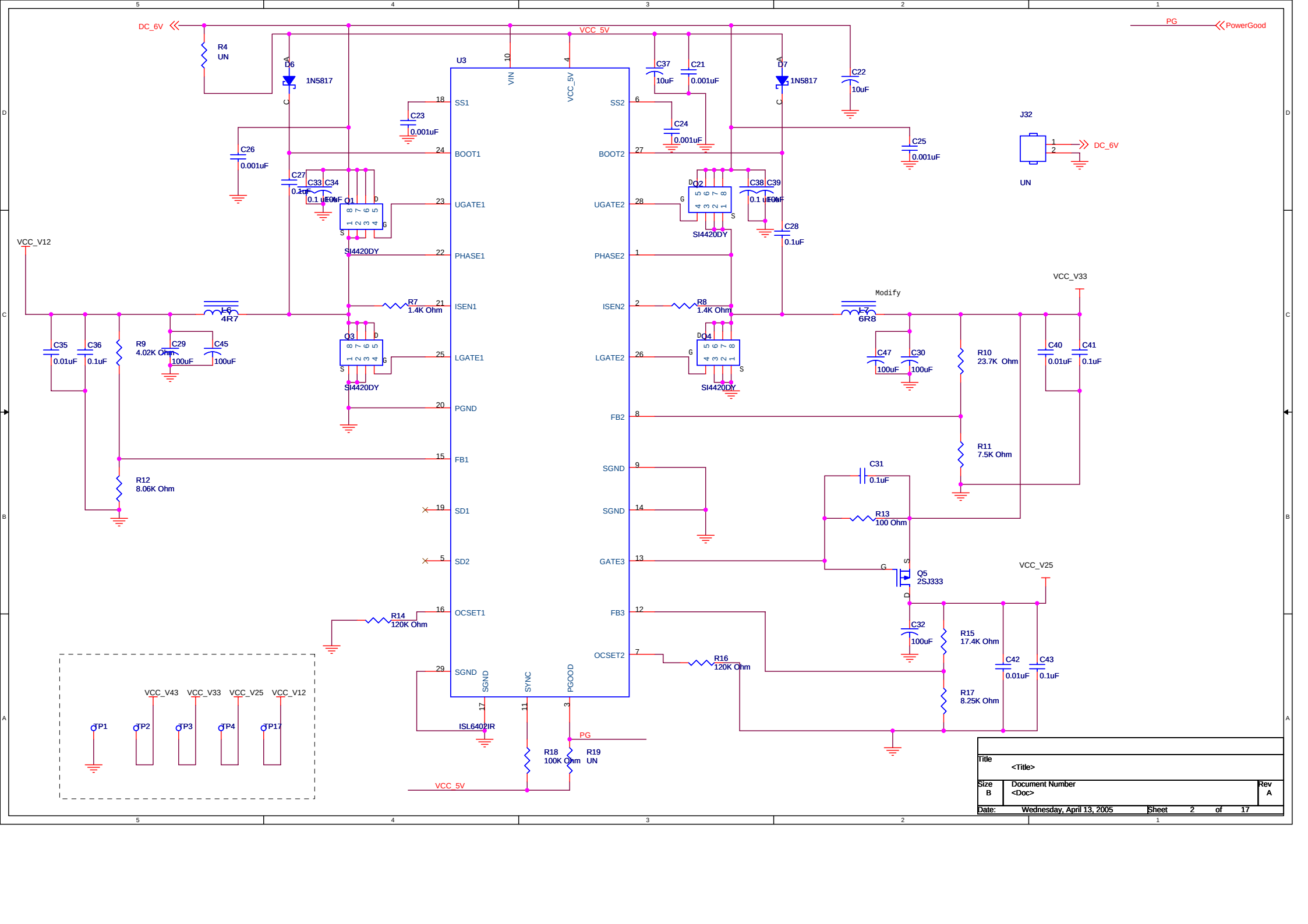
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D7
1N5817
C22
10uF
PG
PowerGood
C23
0.001uF
C24
0.001uF
C25
0.001uF
J32
DC_6V
UN
C26
0.001uF
C27
0.1uF
C33
0.1 uF
C34
0.1uF
Q1
SI4420DY
C38
0.1 uF
C39
0.1uF
Q2
SI4420DY
C28
0.1uF
VCC_V12
SS1
SS2
BOOT1
BOOT2
UGATE1
UGATE2
PHASE1
PHASE2
ISEN1
ISEN2
LGATE1
LGATE2
PGND
FB2
FB1
SGND
SD1
SGND
SD2
GATE3
OCSET1
FB3
OCSET2
SGND
SGND
SYNC
PGOOD
ISL6402IR
L6
4R7
R7
1.4K Ohm
R8
1.4K Ohm
Modify
L7
6R8
VCC_V33
C35
0.01uF
C36
0.1uF
R9
4.02K Ohm
C29
100uF
C45
100uF
Q3
SI4420DY
Q4
SI4420DY
C47
100uF
C30
100uF
R10
23.7K Ohm
C40
0.01uF
C41
0.1uF
R11
7.5K Ohm
R12
8.06K Ohm
C31
0.1uF
R13
100 Ohm
Q5
2SJ333
VCC_V25
C32
100uF
R15
17.4K Ohm
C42
0.01uF
C43
0.1uF
R17
8.25K Ohm
R14
120K Ohm
R16
120K Ohm
R18
100K Ohm
R19
UN
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PG
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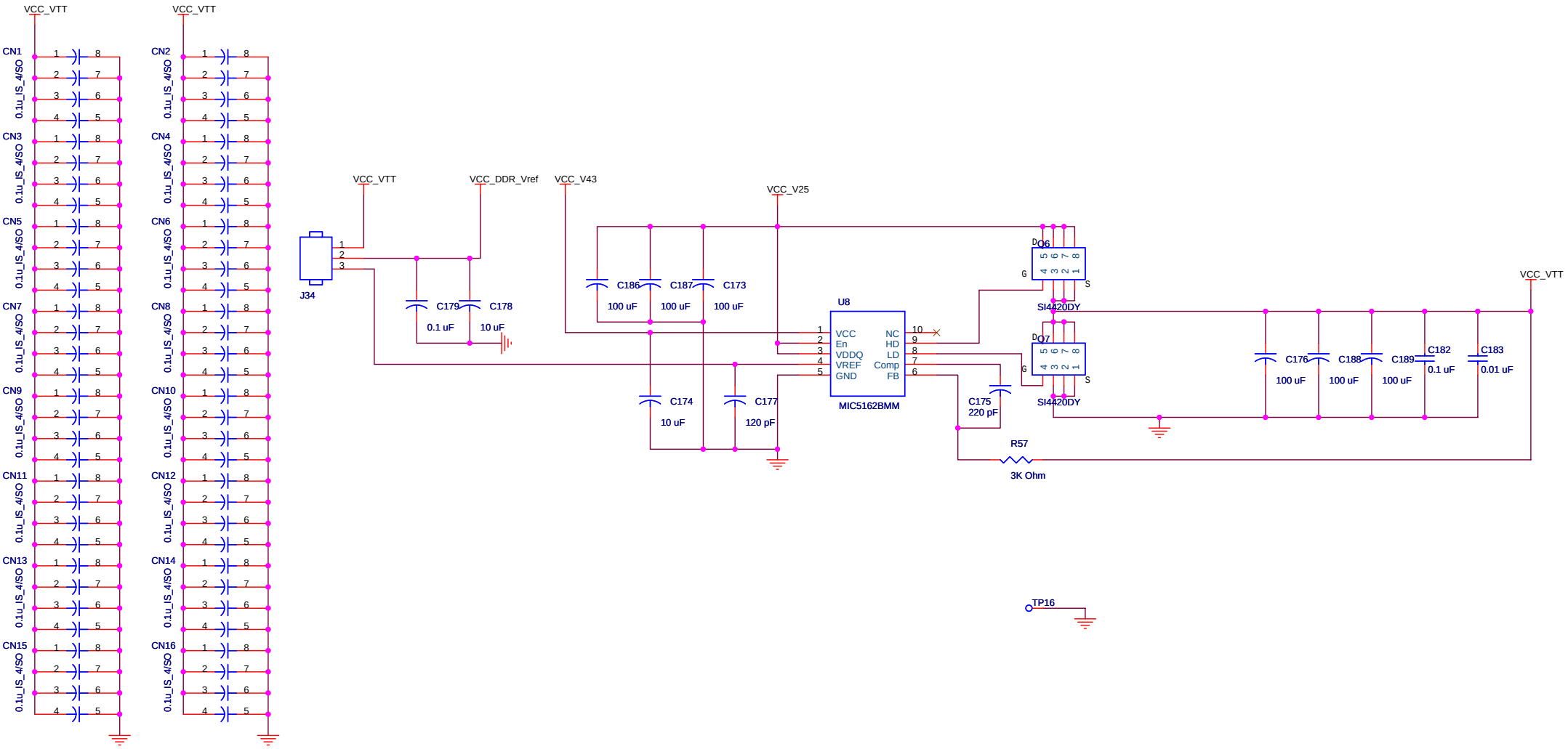
Rev
A
Date:
Wednesday, April 13, 2005
Sheet
2
of
17



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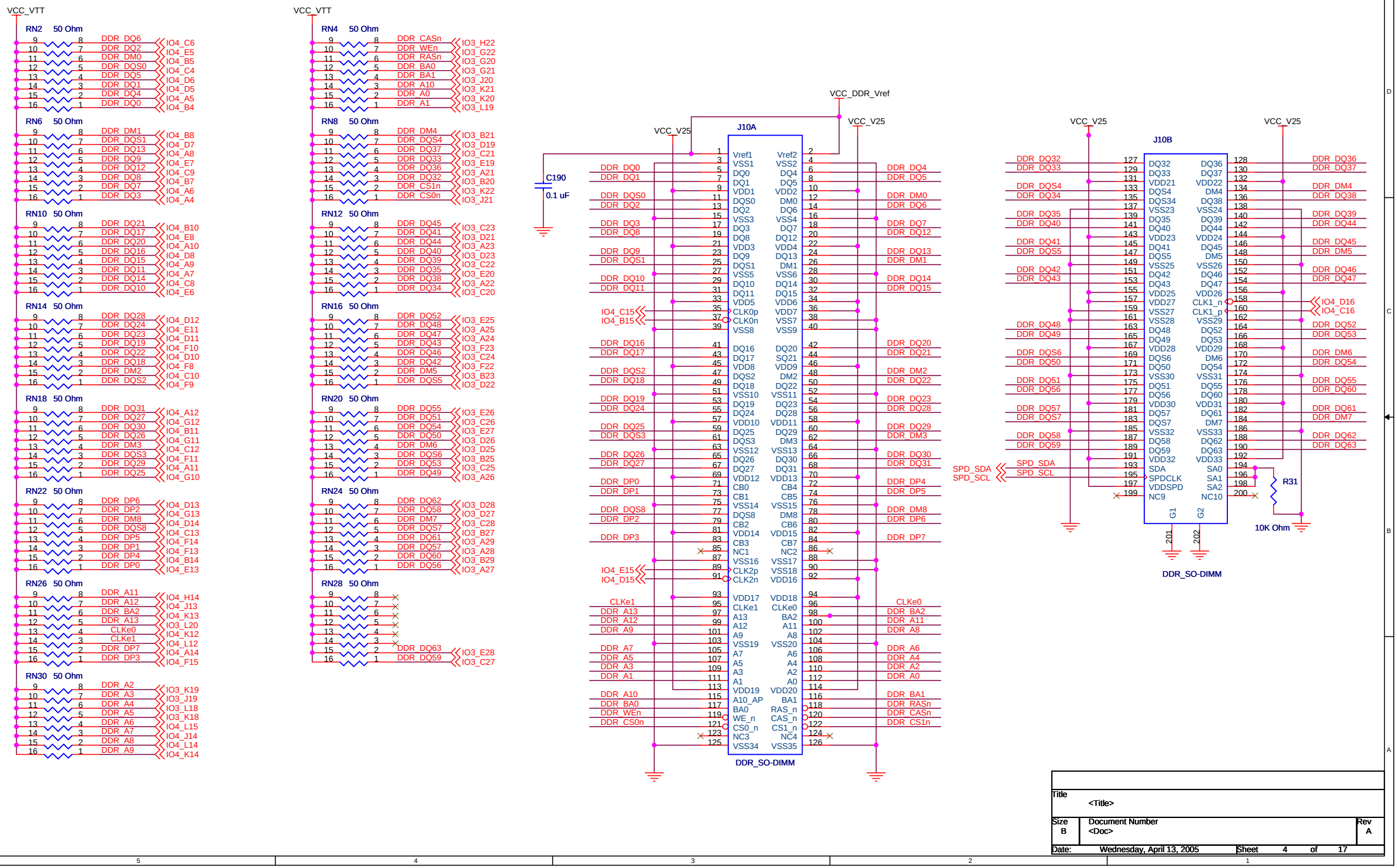
Date: Wednesday, April 13, 2005	Sheet 3 of 17	



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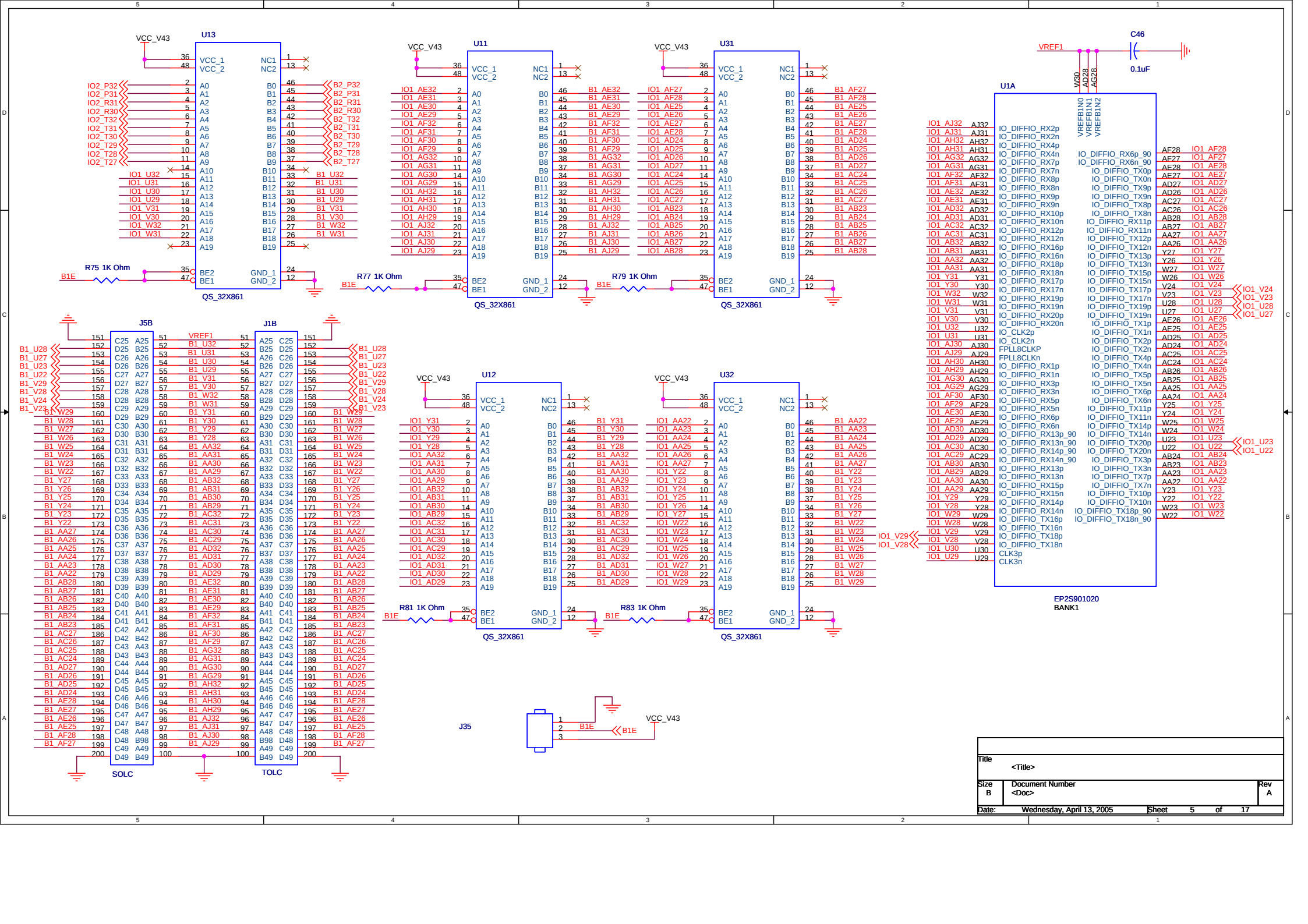
Size B	Document Number <Doc>	Rev A
Date: Wednesday, April 13, 2005	Sheet 4 of 17	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U11
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U31
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C46
VREF1
0.1uF
U1A
EP2S901020
BANK1
J5B
SOLC
J1B
TOLC
U12
R81 1K Ohm
U32
R83 1K Ohm
J35
B1E
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Rev
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Date:
Wednesday, April 13, 2005
Sheet
5
of
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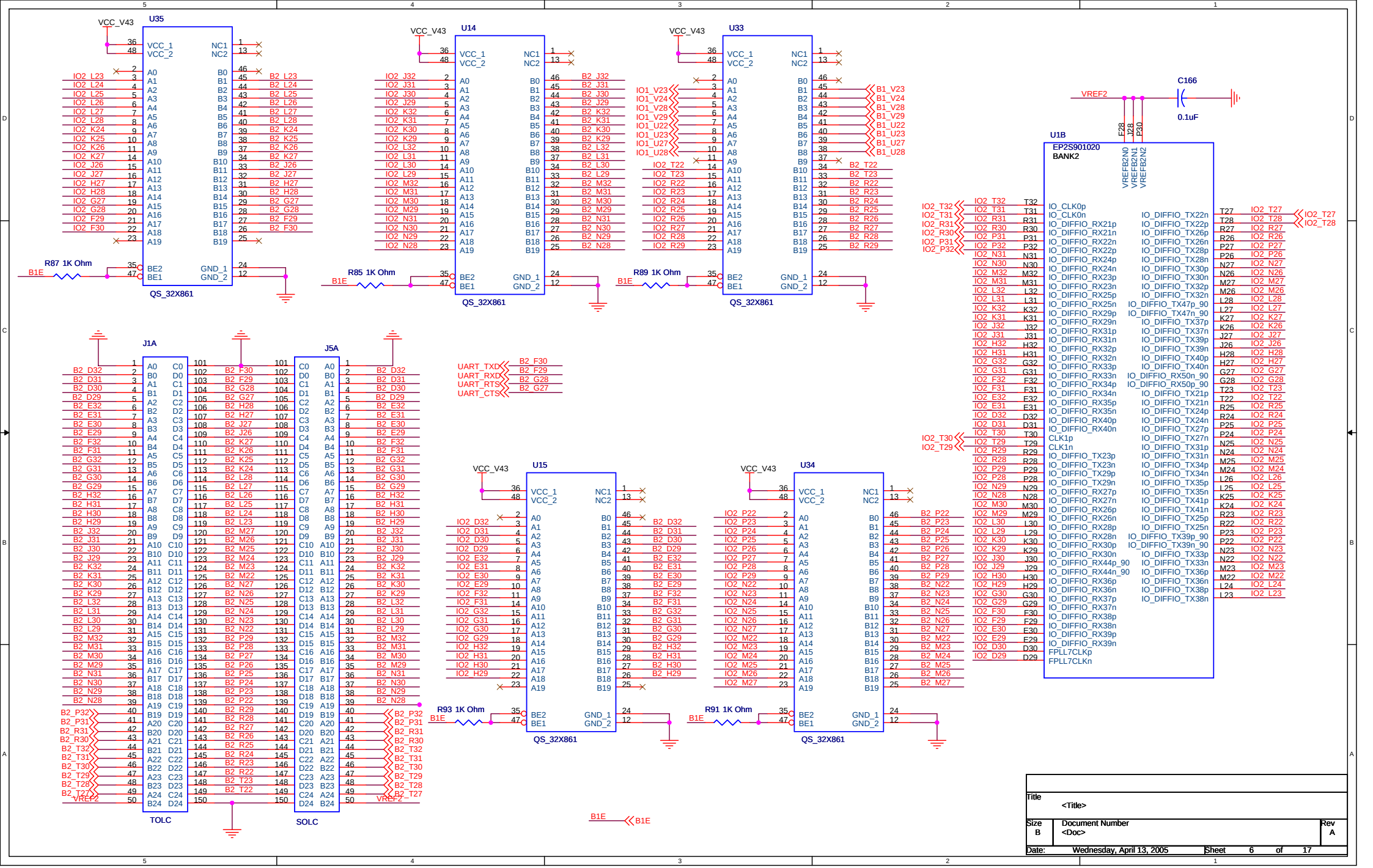
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VCC_1
VCC_2
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NC2
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A1
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A3
A4
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A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
B16
B17
B18
B19
BE2
BE1
GND_1
GND_2
IO2_L23
IO2_L24
IO2_L25
IO2_L26
IO2_L27
IO2_L28
IO2_K24
IO2_K25
IO2_K26
IO2_K27
IO2_J26
IO2_J27
IO2_H27
IO2_H28
IO2_G27
IO2_G28
IO2_F29
IO2_F30
B2_L23
B2_L24
B2_L25
B2_L26
B2_L27
B2_L28
B2_K24
B2_K25
B2_K26
B2_K27
B2_J26
B2_J27
B2_H27
B2_H28
B2_G27
B2_G28
B2_F29
B2_F30
R87 1K Ohm
B1E
QS_32X861
U14
IO2_J32
IO2_J31
IO2_J30
IO2_J29
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IO2_K31
IO2_K30
IO2_K29
IO2_L32
IO2_L31
IO2_L30
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IO2_M31
IO2_M30
IO2_M29
IO2_N31
IO2_N30
IO2_N29
IO2_N28
B2_J32
B2_J31
B2_J30
B2_J29
B2_K32
B2_K31
B2_K30
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B2_L29
B2_M32
B2_M31
B2_M30
B2_M29
B2_N31
B2_N30
B2_N29
B2_N28
R85 1K Ohm
U33
IO1_V23
IO1_V24
IO1_V28
IO1_V29
IO1_U22
IO1_U23
IO1_U27
IO1_U28
IO2_T22
IO2_T23
IO2_R22
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IO2_R27
IO2_R28
IO2_R29
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B1_V24
B1_V28
B1_V29
B1_U22
B1_U23
B1_U27
B1_U28
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B2_R22
B2_R23
B2_R24
B2_R25
B2_R26
B2_R27
B2_R28
B2_R29
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C166
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VREFB2N1
VREFB2N2
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IO_CLK0n
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IO_DIFFIO_RX21n
IO_DIFFIO_RX22n
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CLK1n
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FPLL7CLKn
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IO_DIFFIO_TX30p
IO_DIFFIO_TX30n
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IO_DIFFIO_TX47n_90
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IO2_M23
IO2_M22
IO2_L24
IO2_L23
J1A
J5A
TOLC
SOLC
UART_TXD
UART_RXD
UART_RTS
UART_CTS
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B2_G28
B2_G27
U15
R93 1K Ohm
U34
R91 1K Ohm
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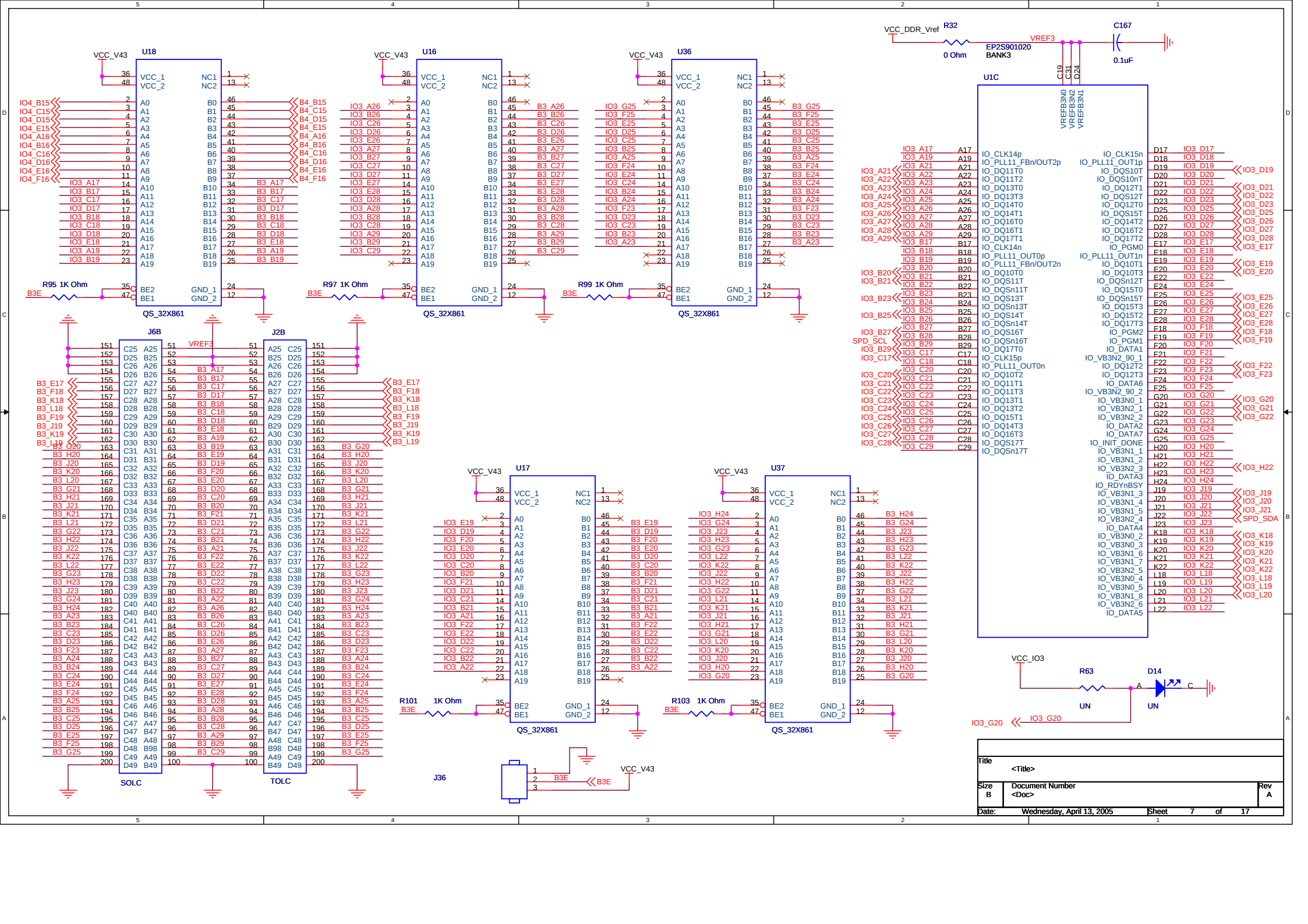
Document Number
<Doc>
Rev
A
Date:
Wednesday, April 13, 2005
Sheet
6
of
17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U17
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J2B
J36
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R32
0 Ohm
VREF3
C167
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R95 1K Ohm
R97 1K Ohm
R99 1K Ohm
R101 1K Ohm
R103 1K Ohm
R63
D14
VCC_IO3
VCC_V43
B3E
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IO_PLL11_FBn/OUT2p
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IO_DQ11T2
IO_DQ13T0
IO_DQ13T3
IO_DQ14T0
IO_DQ14T1
IO_DQ16T0
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IO_DQ17T1
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IO_PLL11_FBn/OUT2n
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IO_DQSn11T
IO_DQ13T
IO_DQSn13T
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IO_DQ14T2
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IO_PGM1
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IO_VB3N2_2
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IO_DATA7
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IO_VB3N1_2
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IO_VB3N1_5
IO_VB3N2_4
IO_DATA4
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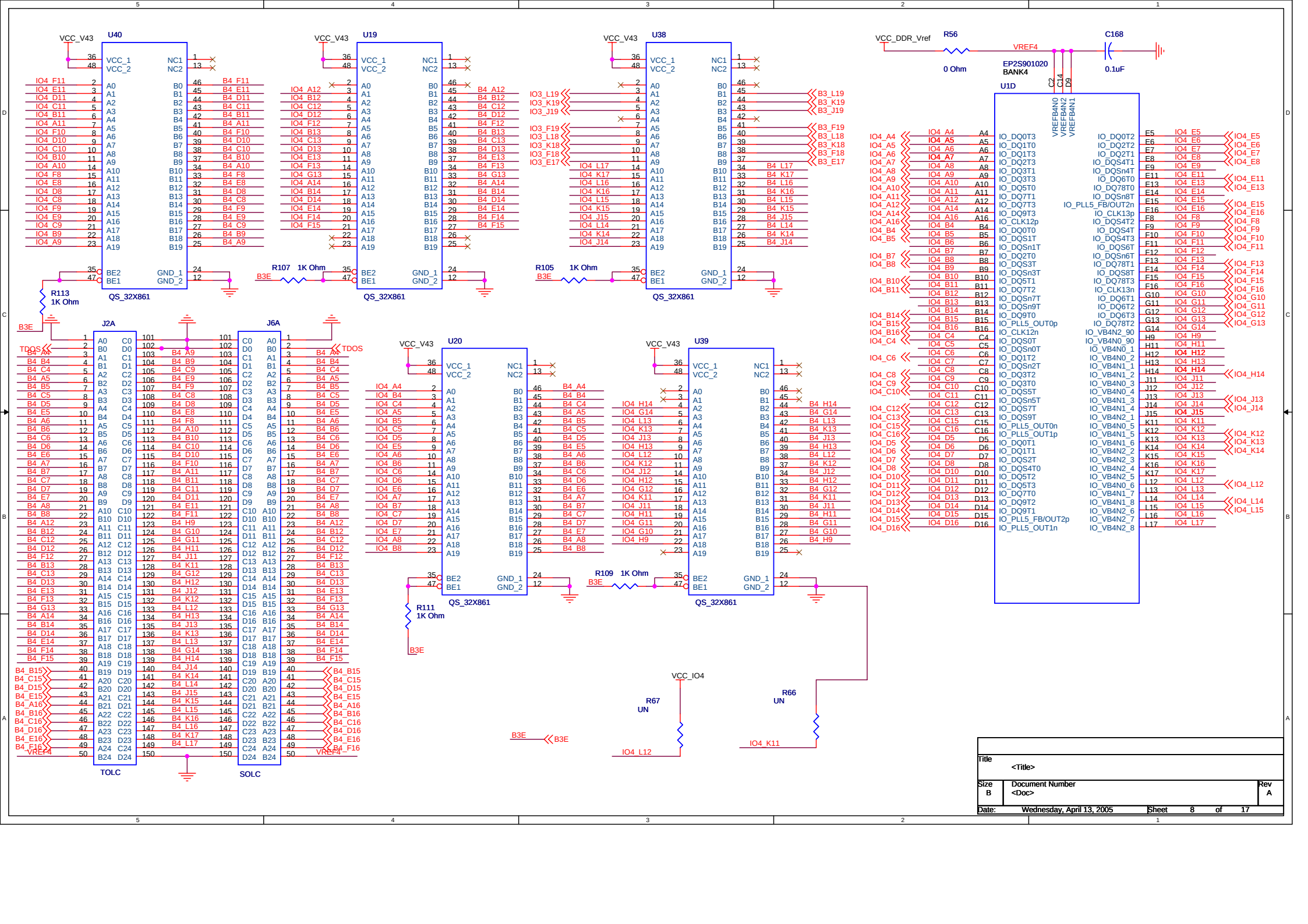
Rev A
Date: Wednesday, April 13, 2005
Sheet 7 of 17



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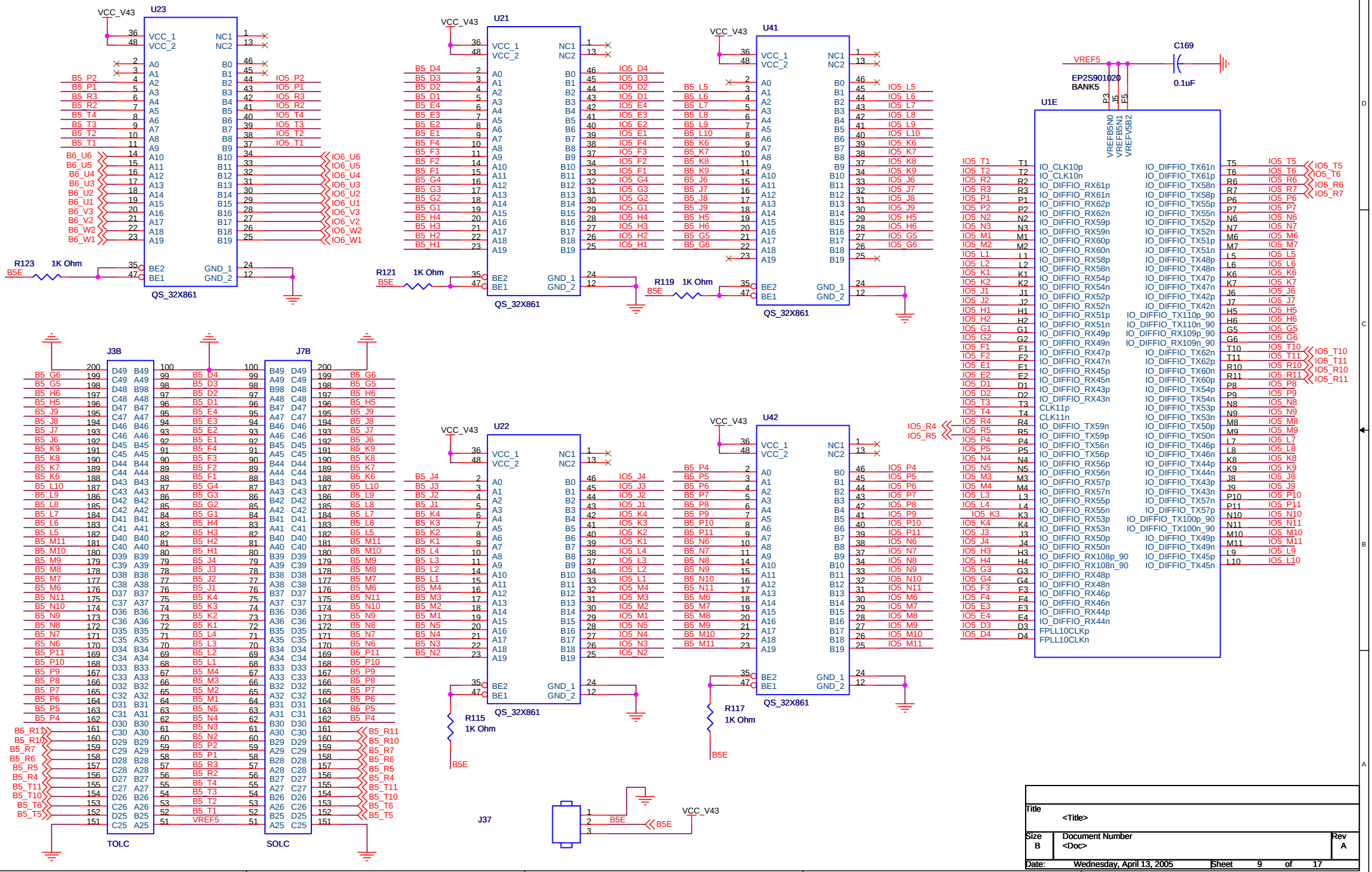
Size B	Document Number <Doc>		Rev A
Date: Wednesday, April 13, 2005	Sheet 8 of 17		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B5E
U21
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IO_DIFFIO_RX61n
IO_DIFFIO_RX62p
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CLK11n
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IO_DIFFIO_TX58n
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IO_DIFFIO_RX109p_90
IO_DIFFIO_RX109n_90
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IO_DIFFIO_TX54n
IO_DIFFIO_TX53p
IO_DIFFIO_TX53n
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IO_DIFFIO_TX50n
IO_DIFFIO_TX49p
IO_DIFFIO_TX49n
IO_DIFFIO_TX45p
IO_DIFFIO_TX45n
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VREFB5N1
VREFV5B2
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J7B
TOLC
SOLC
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R115 1K Ohm
U42
R117 1K Ohm
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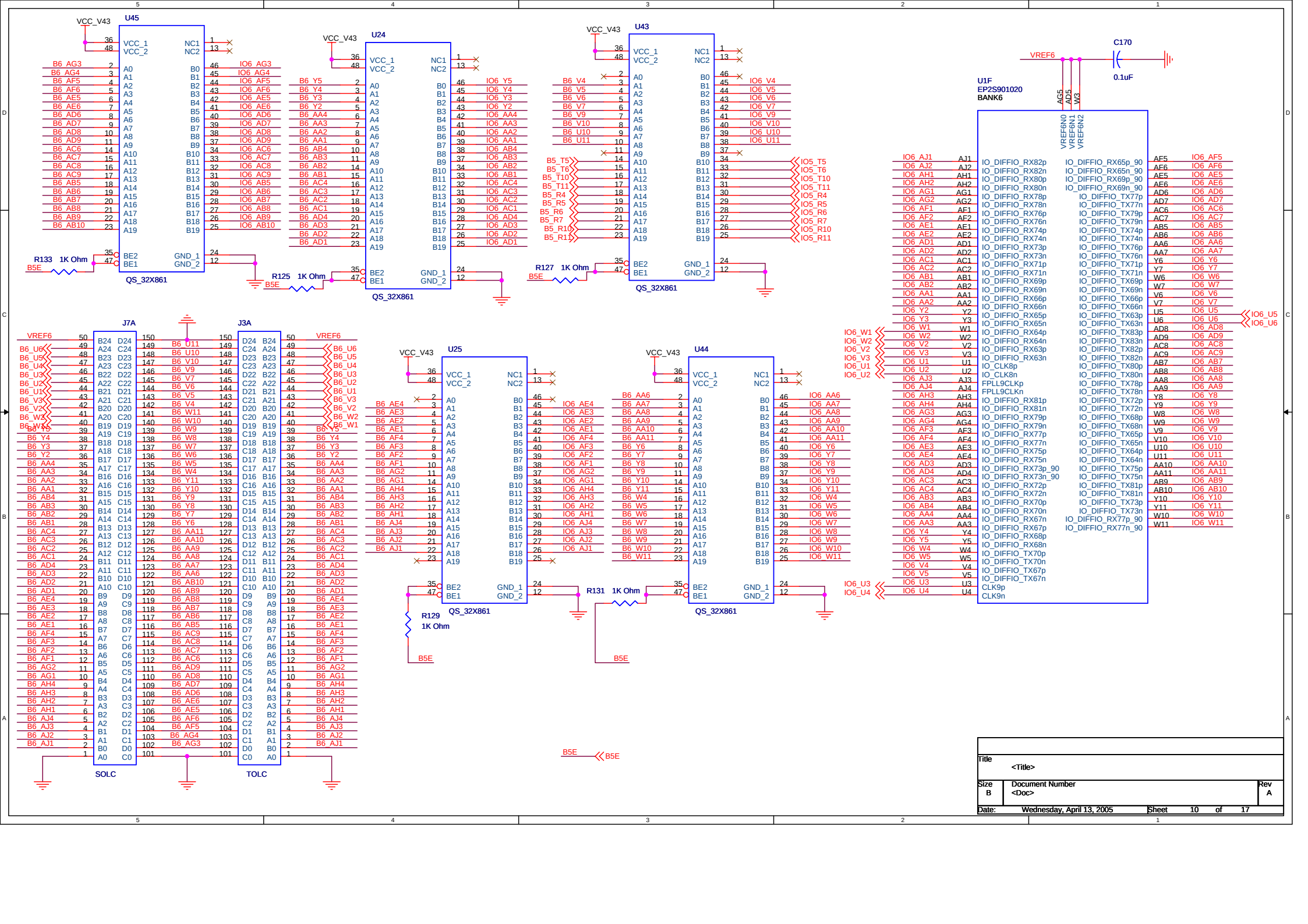
Rev A
Date: Wednesday, April 13, 2005
Sheet 9 of 17



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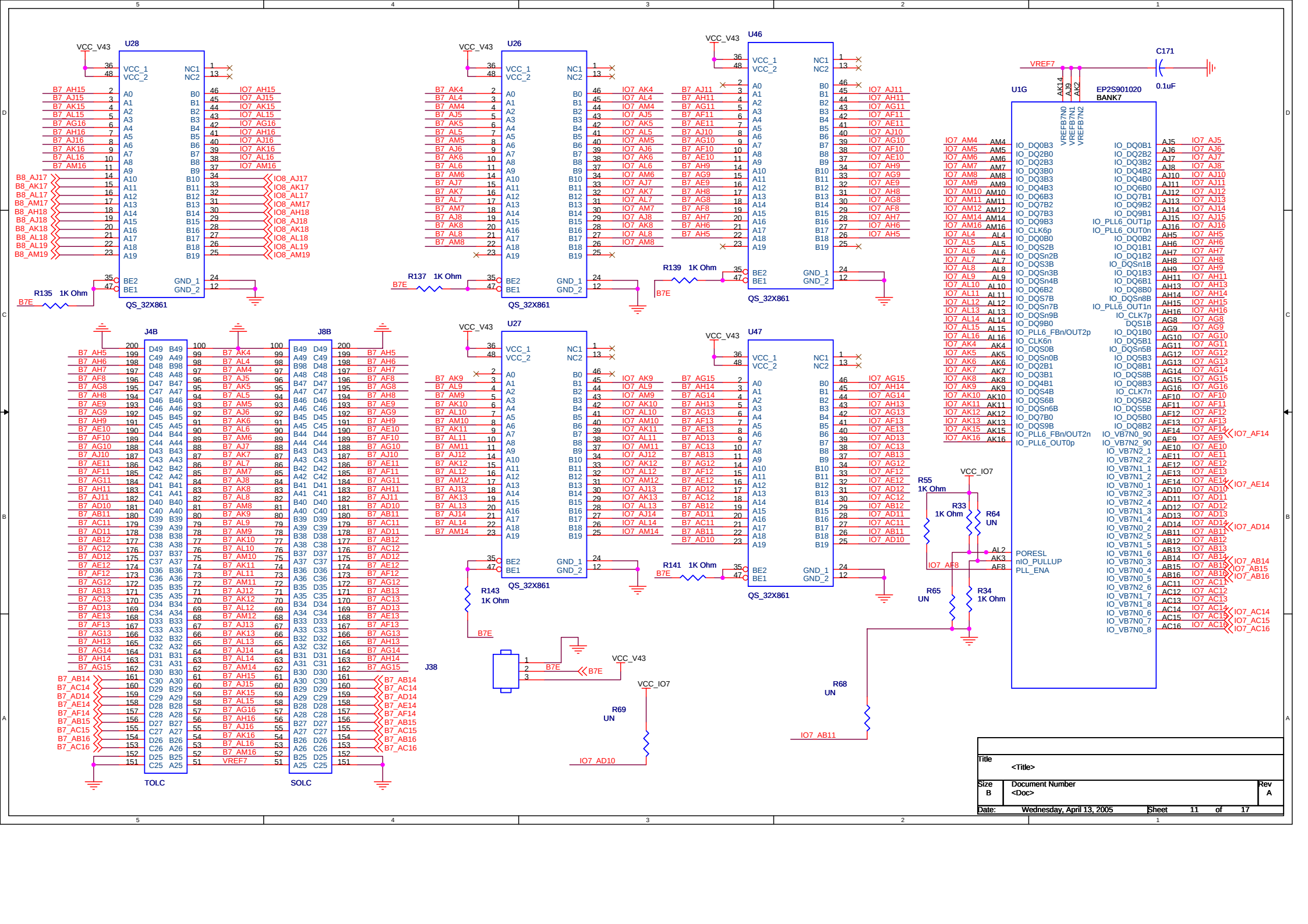
Date: Wednesday, April 13, 2005	Sheet 10 of 17		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U46
U27
U47
U1G
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BANK7
C171
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VREF7
J4B
J8B
J38
TOLC
SOLC
R135 1K Ohm
R137 1K Ohm
R139 1K Ohm
R141 1K Ohm
R143 1K Ohm
R55 1K Ohm
R33 1K Ohm
R64 UN
R65 UN
R34 1K Ohm
R68 UN
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IO7_AD10
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IO7_AF8
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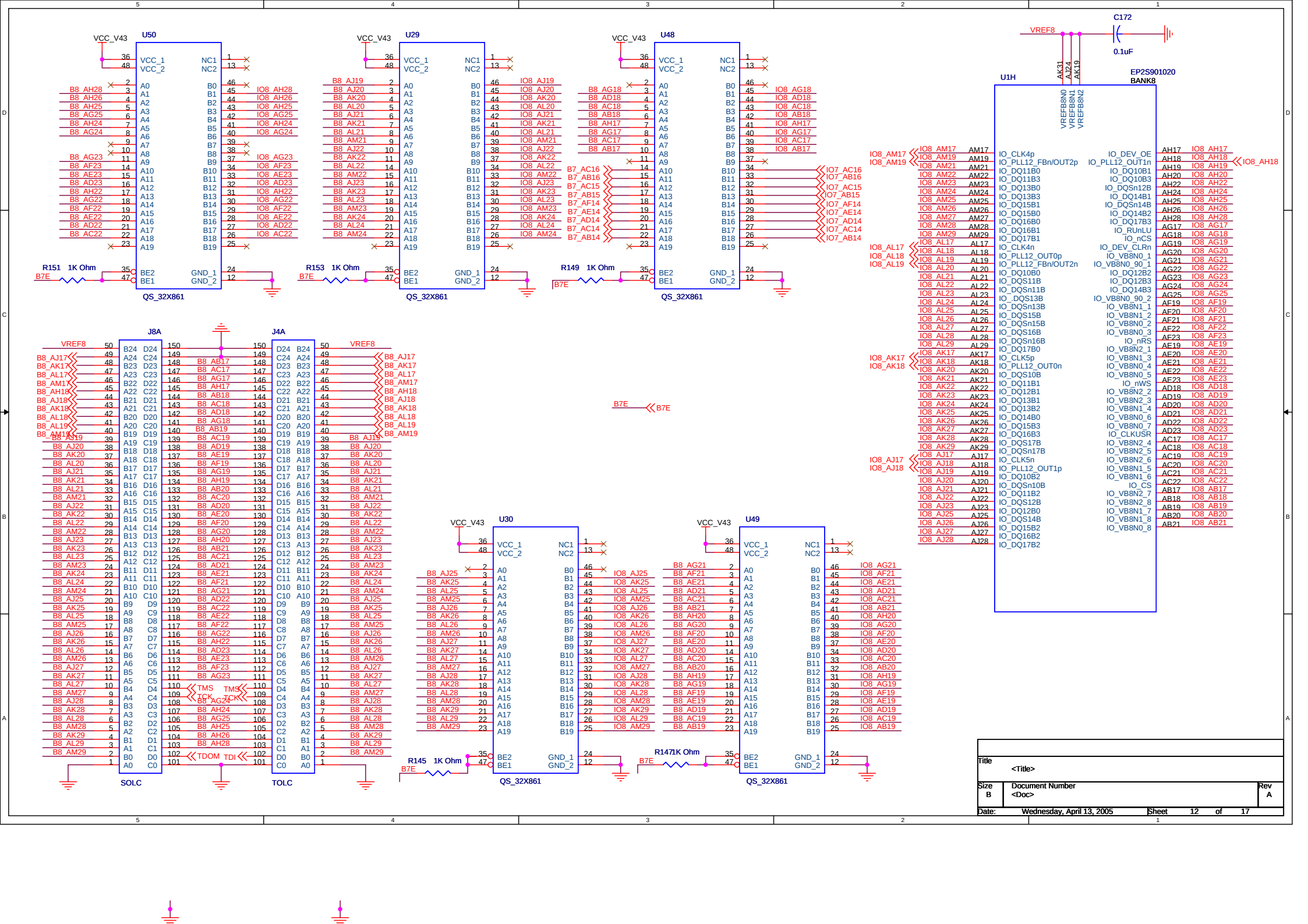
Size B
Document Number
<Doc>
Rev A
Date: Wednesday, April 13, 2005
Sheet 11 of 17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R145 1K Ohm
R147 1K Ohm
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TOLC
U30
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TMS
TCK
TDO
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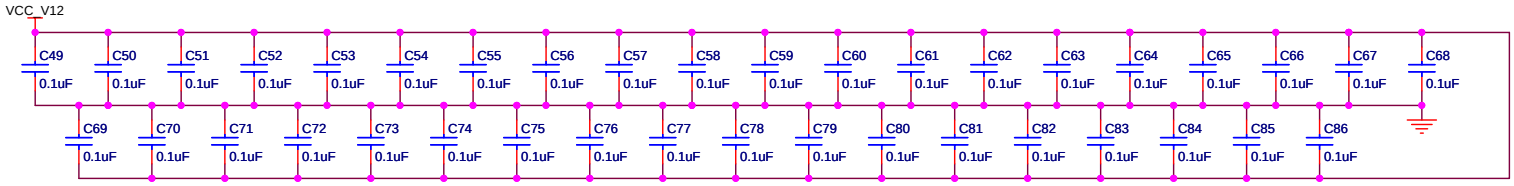
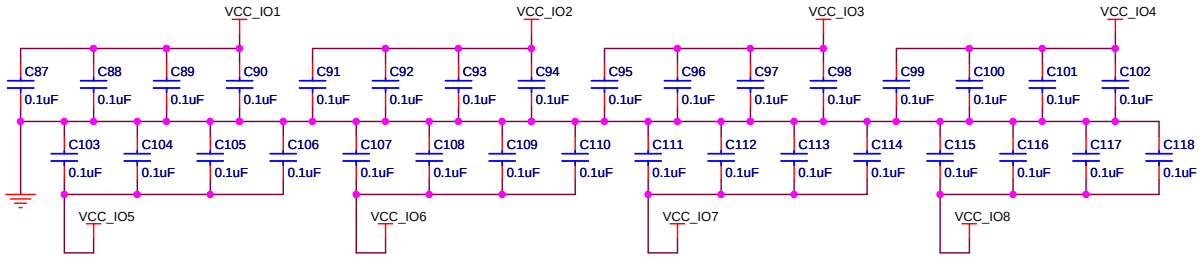
Size B
Document Number
<Doc>
Rev A
Date: Wednesday, April 13, 2005
Sheet 12 of 17

Stratix II Decoupling, VTT Regulators

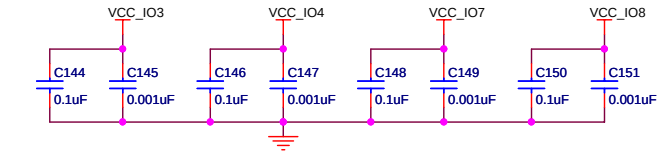
Stratix VCCINT Place those Cap to per VCCINT pin as near as possible



Stratix II VCCIO Place those Cap to per VCCIO pin as near as possible



Stratix II VCC PLL_Out Place those Cap to per VCC PLL_out as near as possible



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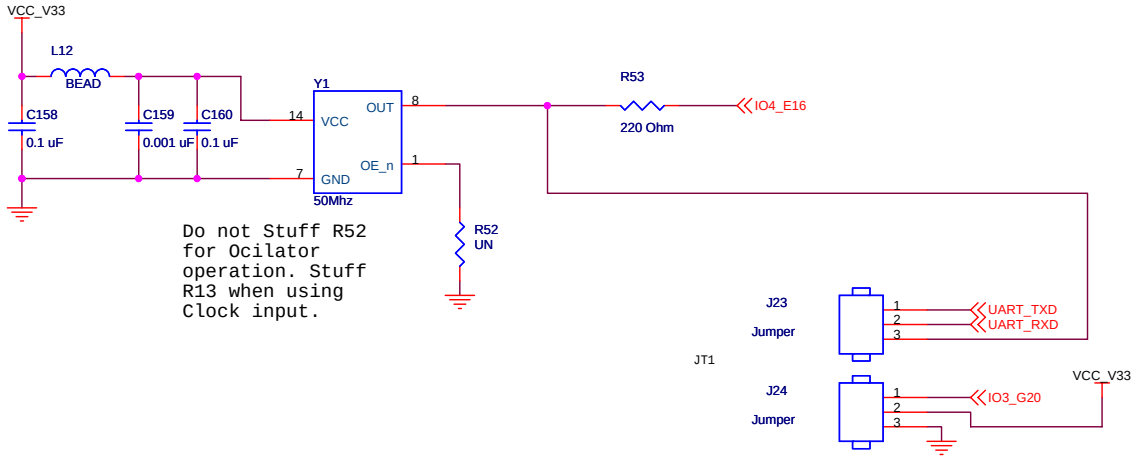
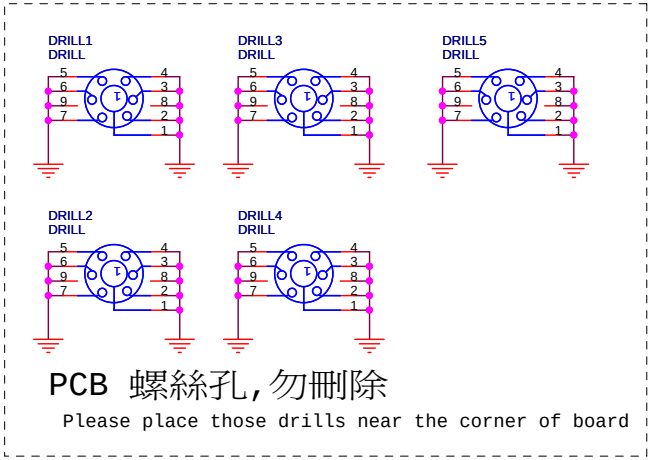
Date: Wednesday, April 13, 2005	Sheet 13 of 17	





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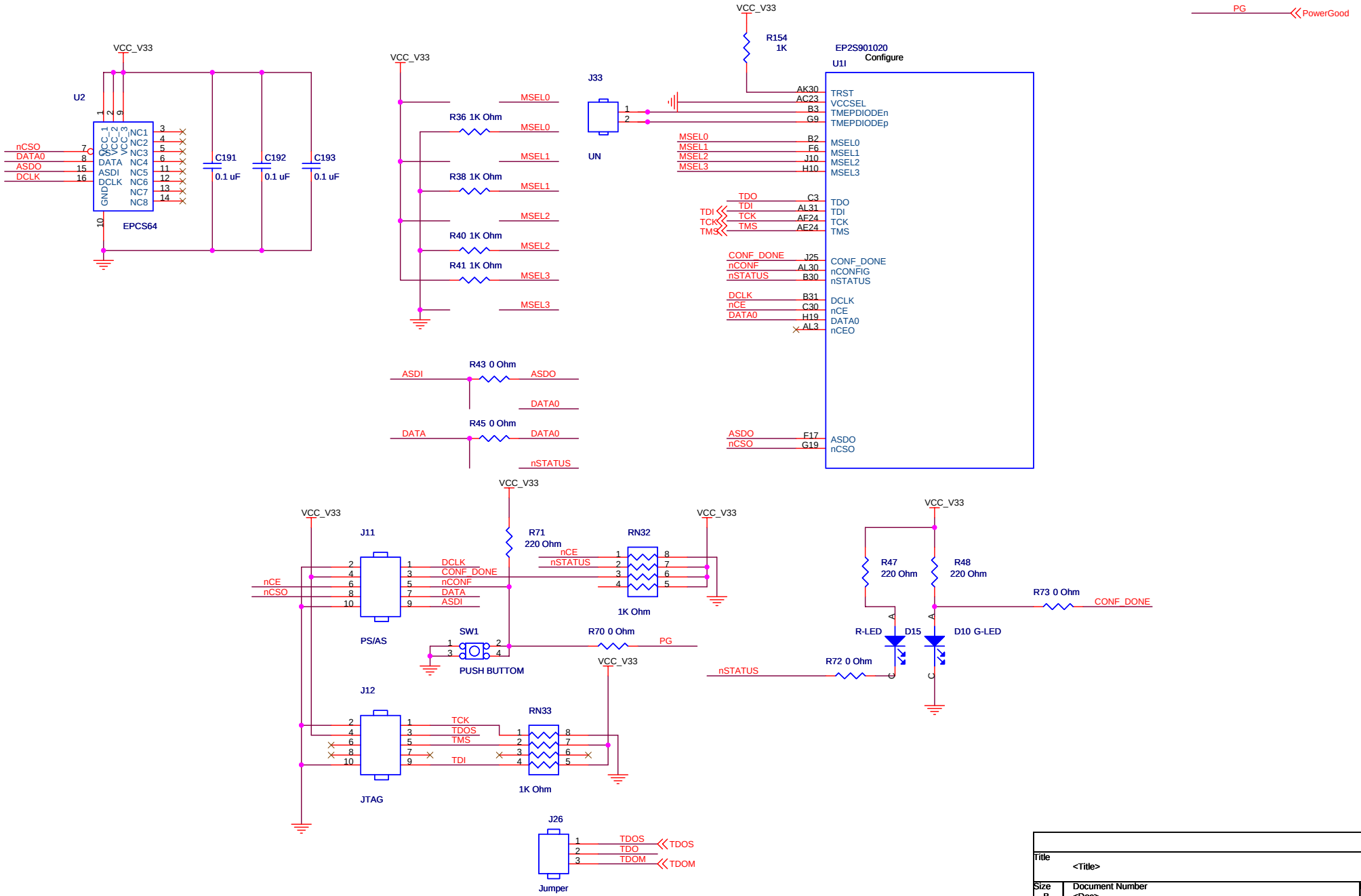
Date: Wednesday, April 13, 2005	Sheet 14 of 17	



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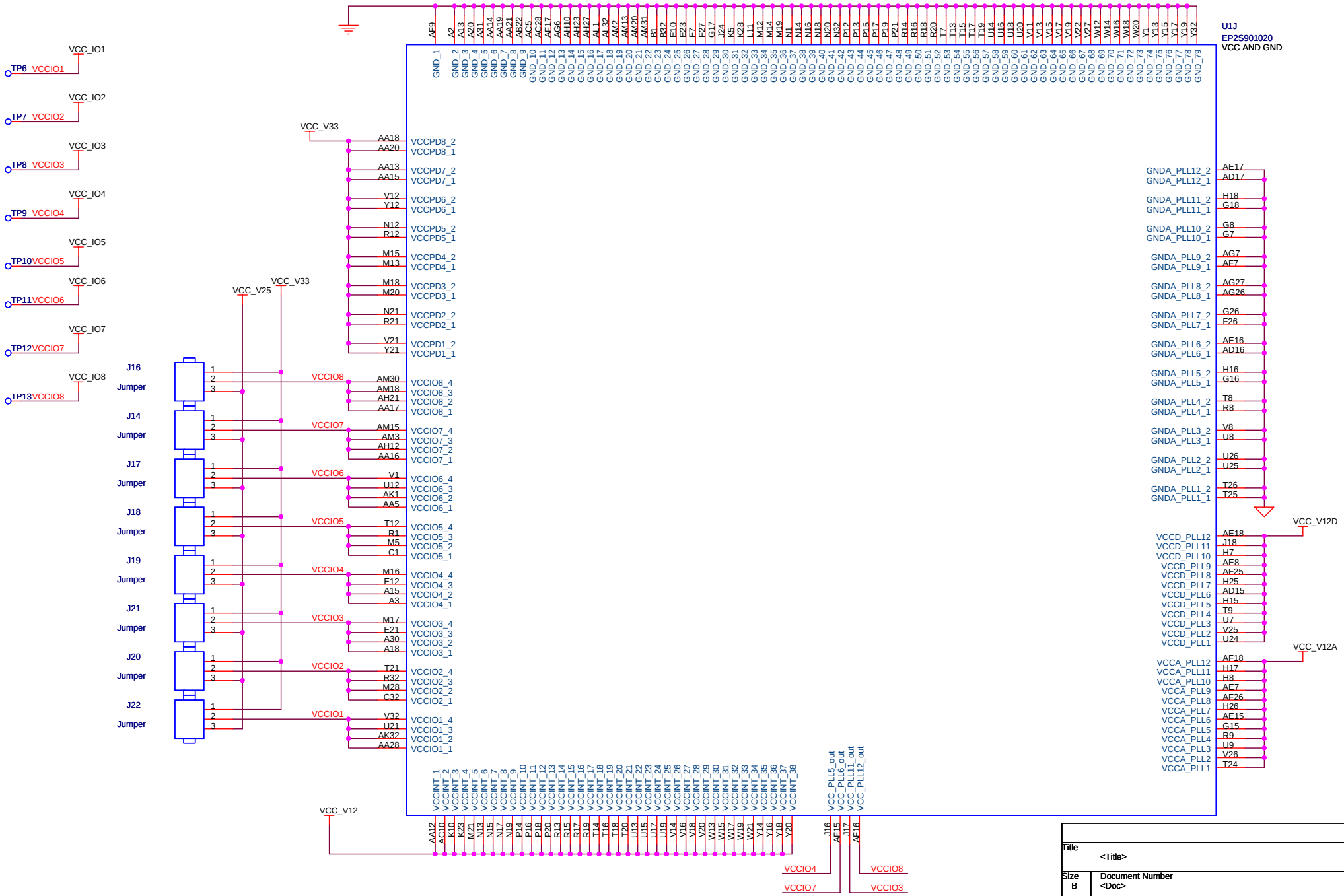
Date: Wednesday, April 13, 2005	Sheet 15 of 17	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VCC AND GND
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VCC_IO2
TP7 VCCIO2
VCC_IO3
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VCC_IO4
TP9 VCCIO4
VCC_IO5
TP10 VCCIO5
VCC_IO6
TP11 VCCIO6
VCC_IO7
TP12 VCCIO7
VCC_IO8
TP13 VCCIO8
VCC_V33
VCC_V25
J16
J14
J17
J18
J19
J21
J20
J22
Jumper
VCCIO8
VCCIO7
VCCIO6
VCCIO5
VCCIO4
VCCIO3
VCCIO2
VCCIO1
VCC_V12
VCC_V12D
VCC_V12A
VCCIO4
VCCIO7
VCCIO8
VCCIO3
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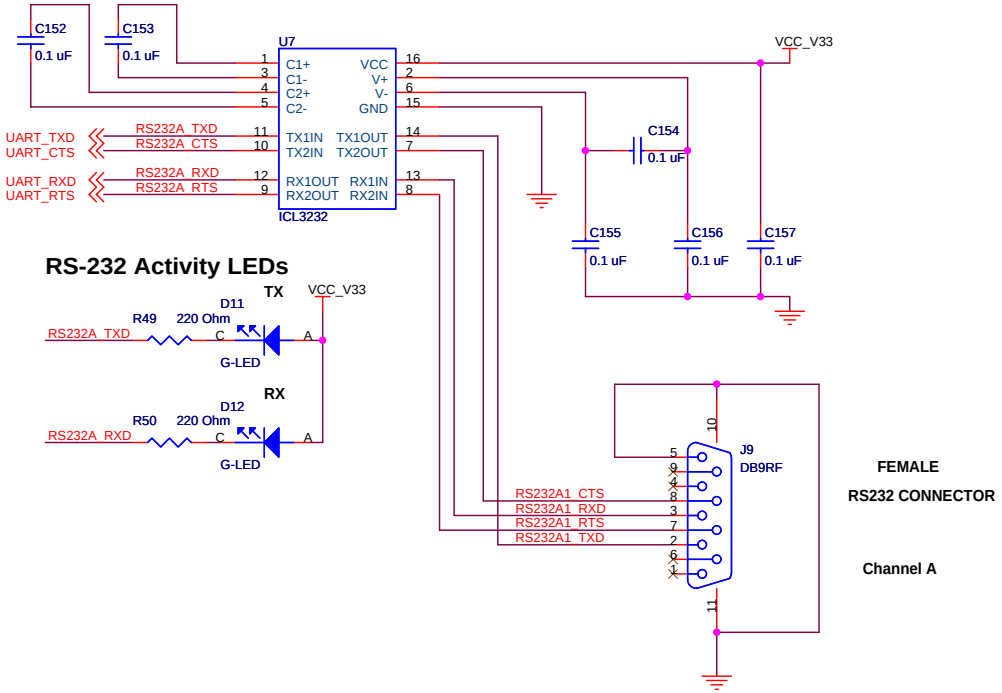
Date: Wednesday, April 13, 2005
Sheet 16 of 17



Title	<Title>	
Size B	Document Number <Doc>	Rev A
Date: Wednesday, April 13, 2005	Sheet 17 of 17	

4.5.I/O Buffer Spec

QUICKSWITCH® PRODUCTS HIGH-SPEED CMOS 20-BIT BUS SWITCH WITH FLOW-THRU PINOUT

IDTQS32X861

FEATURES:

- **Enhanced N channel FET with no inherent diode to Vcc**
- **5Ω bidirectional switches connect inputs to outputs**
- **Zero propagation delay, zero ground bounce**
- **Undershoot clamp diodes on all switch and control inputs**
- **Available in 48-pin QVSOP package**

APPLICATIONS:

- **Hot-swapping, hot-docking**
- **Voltage translation (5V to 3.3V)**
- **Power conservation**
- **Capacitance reduction and isolation**
- **Bus isolation**
- **Clock gating**

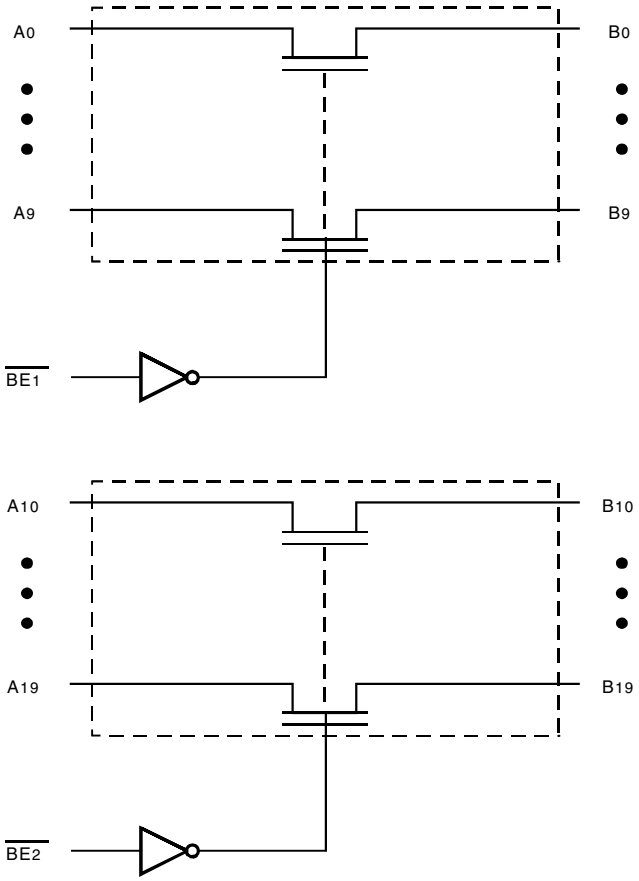
DESCRIPTION:

The QS32X861 provides two sets of ten high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS32X861 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{BE}n$) signals turn the switches on.

The QS32X861 bus switch is ideal for switching digital buses, as well as for hotplug buffering and 5V to 3V conversion.

The QS32X861 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



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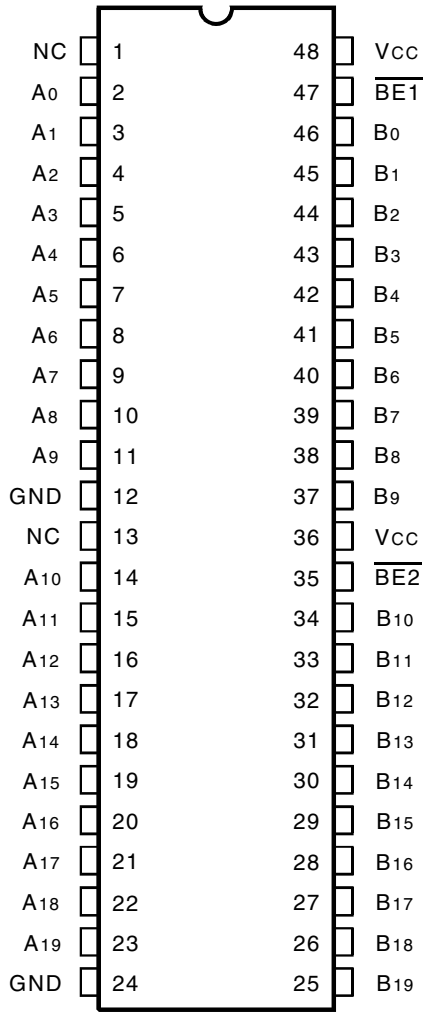
PIN CONFIGURATION



QVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Supply Voltage to Ground	–0.5 to +7	V
V_{TERM}(3)	DC Switch Voltage Vs	–0.5 to +7	V
V_{TERM}(3)	DC Input Voltage V_{IN}	–0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤ 20ns)	–3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation (T_A = 85°C)	0.5	W
T_{STG}	Storage Temperature	–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins	Typ.	Max.(1)	Unit
Control Pins	3	5	pF
Quickswitch Channels (Switch OFF)	5	7	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
A_0 - A_{19}	I/O	Bus A
B_0 - B_{19}	I/O	Bus B
$\overline{BE}n$	I	Bus Enable

FUNCTION TABLE(1)

$\overline{BE1}$	$\overline{BE2}$	A_0 - A_9	A_{10} - A_{19}	Function
L	L	B_0 - B_9	B_{10} - B_{19}	Connect
L	H	B_0 - B_9	Z	Connect
H	L	Z	B_{10} - B_{19}	Connect
H	H	Z	Z	Disconnect

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Z = High-Impedance

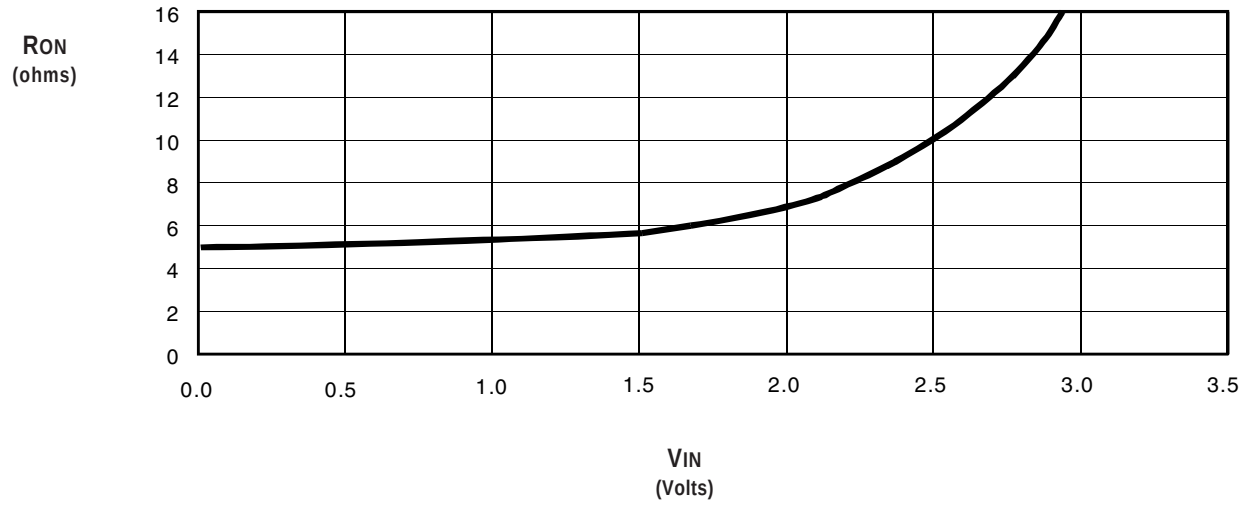
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH for Control Pins	2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
I_{IN}	Input LeakageCurrent (Control Inputs)	0V ≤ V_{IN} ≤ V_{CC}	—	±0.01	±1	µA
I_{OZ}	Off-State Output Current (Hi-Z)	0V ≤ V_{OUT} ≤ V_{CC}, Switches OFF	—	±0.01	±1	µA
R_{ON}	Switch ON Resistance	V_{CC} = Min., V_{IN} = 0V, I_{ON} = 30mA	—	5	7	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} =15mA	—	10	15	
V_P	Pass Voltage[2]	V_{CC} = 5V, I_{OUT} = -5µA	3.7	4	4.2	V

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Pass Voltage is guaranteed but not production tested.

TYPICAL ON RESISTANCE vs V_{IN} AT V_{CC} = 5V



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Typ[2]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc, f = 0	0.2	6	µA
ΔI_{CC}	Power Supply Current per Control Input HIGH[3]	V_{CC} = Max., V_{IN} = 3.4V, f = 0	—	2.5	mA
I_{CCD}	Dynamic Power Supply Current per MHz[4]	V_{CC} = Max., A and B pins open $\overline{BE}n$ Control Input Toggling at 50% Duty Cycle	—	0.25	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, 25°C ambient.
3. Per TLL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to ΔIcc.
4. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B pins generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

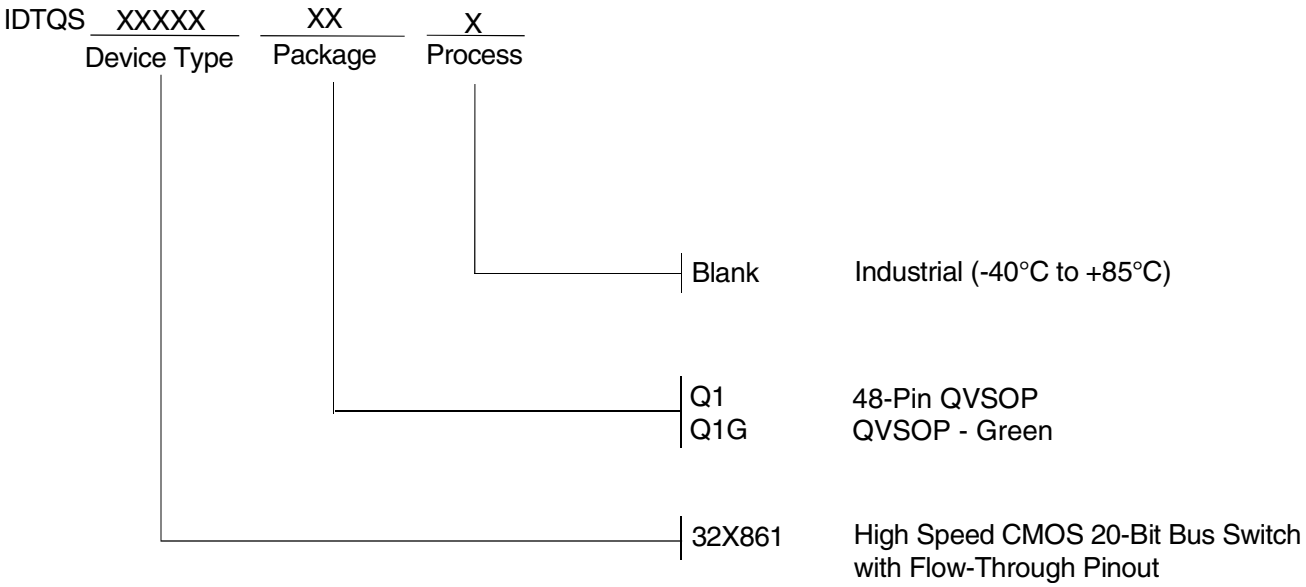
T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%;

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Parameter	Min.[1]	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] An to/from Bn	—	0.25	—	ns
t_{PZH} t_{PZL}	Switch Turn-on Delay $\overline{BE}n$ to An/Bn	1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch Turn-off Delay[2] $\overline{BE}n$ to An/Bn	1.5	—	5.5	ns

NOTES:
1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

ORDERING INFORMATION



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5. Reference

TAB. 1 STRATIX DEVICE FAMILY 17
TAB. 2 STRATIX II PACKAGE OFFERINGS & USERS I/O COUNTS 17
TAB. 3 DEDICATE PIN 20
TAB. 4 NOT COMPATIBLE PINS IN ALL FAMILY 21
TAB. 5 JP1 & JP5 (I) 23
TAB. 6 JP1 & JP5 (II) 24
TAB. 7 JP2 & JP6 (I) 25
TAB. 8 JP2 & JP6 (II) 26
TAB. 9 JP3 & JP7(I) 27
TAB. 10 JP3 & JP7 (II) 28
TAB. 11 JP4 & JP8 (I) 29
TAB. 12 JP4 & JP8 (II) 30
TAB. 13 UART IN GFEC STRATIX II DEVELOPMENT BOARD 34
TAB. 14 GLOBAL CLOCK IN GFEC STRATIX II DEVELOPMENT BOARD 35
TAB. 15 CONTAINS DETAILS ABOUT QUARTUS® II SOFTWARE VERSION 4.2 OPERATING SYSTEM (OS) SUPPORT. 38
TAB. 16 QUARTUS II SUPPORT STRATIX II TIMING MODEL & POF 39
TAB. 17 3RD SUPPORT STRATIX II DEVICE FAMILY 39

FIG. 1 STRATIX II EP2S60 FLOORPLAN 9
FIG. 2 OUTSIDE VIEW OF GFEC STRATIX II DEVELOPMENT BOARD 15
FIG. 3 STRUCTURAL DIAGRAM OF GFEC STRATIX II DEVELOPMENT BOARD 16

Version Change Record

V0.50	Alpha Version
V0.80	Beta Version
V0.90	Pre-Release 1
V1.0	The first version manual
V2.0	The Board Version C & Bug fixed